

FUNCTION GENERATOR NEST

TERMINATION

COMBINER

FG1 B0

FG2 B4

FG3 B8

FG4				B6	
4	A3	3	A2	2	A1
1	A0	6	A5	5	A4

FG5 C0

FG6 C4

SPARE

FG SEL INTENS 9B BLUE 9A GREEN 99 RED 98

FG SEL DEPTH 97 VERT 96 WIDTH 95 HORIZ 94

FG SEL SPARE 93 SPARE 92 HBLW 91 HBLST 90

MDAC
CIC-1-1
MDAC
CIC-1-1

1
3
5
7
9
11
12
13
15
17
19
21
23
25

RPU NEST 3

FUNCTION GENERATOR + COMBINER

11 FG 4				9 FG 3				7 FG 2				5 FG 1				3 COMBINER							
1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1	+5	GND	62	1			62
2	+5	GND	63		+5	GND			+5	GND			+5	GND			+5	GND		2			63
3	RPU STROBE	-5	64																	3			64
4	RPU WRITE	SYNCH SRT	65																	4			65
5	H SYNCH	F SYNCH	66	5			66	5			66	5			66	5			66	5			66
6	S SYNCH	V SYNCH	67																	6			67
7	CON 1	SYNCH SRT	68																	7			68
8	CON 0	RPU TO SER	69																	8			69
9	BUSSE R	RPUA 0	70																	9			70
10	RPU 0 0	RPUA 1	71	10			71	10			71	10			71	10			71	10			71
11	RPU 0 1	RPUA 2	72																	11			72
12	RPU 0 2	RPUA 3	73																	12			73
13	RPU 0 3	RPUA 4	74																	13			74
14	RPU 0 4	RPUA 5	75																	14			75
15	RPU 0 5	RPUA 6	76	15			76	15			76	15			76	15			76	15			76
16	RPU 0 6	RPUA 7	77																	16			77
17	RPU 0 7	RPUA 8	78																	17			78
18	RPU 0 8	RPUA 9	79																	18			79
19	RPU 0 9	RPUA 10	80																	19			80
20	RPU 0 10	RPUA 11	81	20			81	20			81	20			81	20			81	20			81
21	RPU 0 11	RPUA 12	82																	21			82
22	RPU 0 12	RPUA 13	83																	22			83
23	RPU 0 13	RPUA 14	84																	23			84
24	RPU 0 14	RPUA 15	85																	24			85
25	RPU 0 15	VBLANK	86	25			86	25			86	25			86	25			86	25			86
26	RPU 0 16	MCLK	87																	26			87
27	SAME 1	SAME 2	88																	27			88
28			89																	28			89
29	FG 4 0 7		90		FG 3 0 7				FG 2 0 7				FG 1 0 7							29			90
30	FG 4 0 6		91	30	FG 3 0 6		91	30		FG 2 0 6		91	30		FG 1 0 6		91	30		30			91
31	FG 4 0 5		92		FG 3 0 5				FG 2 0 5				FG 1 0 5				FG 2 0 6	FG 1 0 5		31			92
32	FG 4 0 4		93		FG 3 0 4				FG 2 0 4				FG 1 0 4				FG 2 0 5	FG 1 0 4		32			93
33	FG 4 0 3		94		FG 3 0 3				FG 2 0 3				FG 1 0 3				FG 2 0 4	FG 1 0 3		33			94
34	FG 4 0 2		95		FG 3 0 2				FG 2 0 2				FG 1 0 2				FG 2 0 3	FG 1 0 2		34			95
35	FG 4 0 1		96	35	FG 3 0 1		96	35		FG 2 0 1		96	35		FG 1 0 1		96	35		35			96
36	FG 4 0 0		97		FG 3 0 0				FG 2 0 0				FG 1 0 0				FG 2 0 1	FG 1 0 0		36			97
37	LDAC 4		98		LDAC 3				LDAC 2				LDAC 1				FG 2 0 0	LDAC 1	TWISTED PAIR ON ALL LDAC SIGNALS	37			98
38			99														LDAC 2			38			99
39			100																	39			100
40			101	40			101	40			101	40			101	40		FG 2 0 7	FG 2 0 6	101	40		101
41			102															FG 2 0 5		41			102
42			103															FG 2 0 4		42			103
43			104															FG 2 0 3		43			104
44			105															FG 2 0 2		44			105
45			106	45			106	45			106	45			106	45		FG 2 0 1	FG 2 0 0	106	45		106
46			107															FG 2 0 0		46			107
47			108															LDAC 2		47			108
48			109															LDAC 3		48			109
49			110																	49			110
50			111	50			111	50			111	50			111	50				111	50		111
51	V4OUT		112	51	V3OUT			V2OUT			V1OUT				Vcom 1					51			112
52			113												Vcom 2					52			113
53	+15		114	53	+15			+15			+15				+15					53			114
54			115																	54			115
55	-15		116	55	-15		116	55	-15		116	55	-15		116	55	-15			116	55		116
56			117																	56			117
57	GND I		118		GND I			GND I			GND I				GND I					57			118
58			119																	58			119
59			120																	59			120
60	+5	GND	121	60	+5	GND	121	60	+5	GND	121	60	+5	GND	121	60	+5	GND	121	60			121
61	+5	GND	122	61	+5	GND	122	61	+5	GND	122	61	+5	GND	122	61	+5	GND	122	61			122

— DENOTES SIGNALS BUSSED ACROSS BACKPLANE

RPU NEST 1

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
0	0 INTENSITY CFG AMP	OFF	MD	8	+10	HF	CIC-1-4
1	1 RED 1	↓	↓	↓	↓	↓	↓
2	2 GREEN 1	↓	↓	↓	↓	↓	↓
3	3 BLUE 1	↓	↓	↓	↓	↓	↓
8	10 IC 1 (AF-BE)	OFF	MD	12	+10	HF	CIC-1-1
9	11 IC 2 (BI-AJ)	↓	↓	↓	↓	↓	↓
A	12 IC 3 (JE-FI)	↓	↓	↓	↓	↓	↓
B	13 SPARE	↓	↓	↓	↓	↓	↓
10	20 INTENSITY	BIN	D	8	+10	LF	CIC-5
11	21 RED 1	↓	↓	↓	↓	↓	↓
12	22 GREEN 1	↓	↓	↓	↓	↓	↓
13	23 BLUE 1	↓	↓	↓	↓	↓	↓
14	24 RED 2	↓	↓	↓	↓	↓	↓
15	25 GREEN 2	↓	↓	↓	↓	↓	↓
16	26 BLUE 2	↓	↓	↓	↓	↓	↓
17	27 RED 3	↓	↓	↓	↓	↓	↓
18	30 GREEN 3	BIN	D	8	+10	LF	CIC-5
19	31 BLUE 3	↓	↓	↓	↓	↓	↓
1A	32 RED 4	↓	↓	↓	↓	↓	↓
1B	33 GREEN 4	↓	↓	↓	↓	↓	↓
1C	34 BLUE 4	↓	↓	↓	↓	↓	↓
1D	35 RED 5	↓	↓	↓	↓	↓	↓
1E	36 GREEN 5	↓	↓	↓	↓	↓	↓
1F	37 BLUE 5	↓	↓	↓	↓	↓	↓

RPU NEST 1

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
20	40 AUX 1	OFF	D	12	<u>+10</u>	LF	CIC-1-2
21	41 AUX 2	↓	↓	↓	↓	↓	↓
22	42 AUX 3	↓	↓	↓	↓	↓	↓
23	43 AUX 4	↓	↓	↓	↓	↓	↓
28	50 AUX 5	OFF	D	12	<u>+10</u>	LF	CIC-1-2
29	51 AUX 6	↓	↓	↓	↓	↓	↓
2A	52 SPARE	↓	↓	↓	↓	↓	↓
2B	53 SPARE	↓	↓	↓	↓	↓	↓
30-37	60-67	} SPARES					
38-3F	70-77						

PCB	CIRC	
1	3	CIC-1-1
2	6	CIC-1-2
1	4	CIC-1-4
2	16	CIC-5
6		

RPU NEST 2

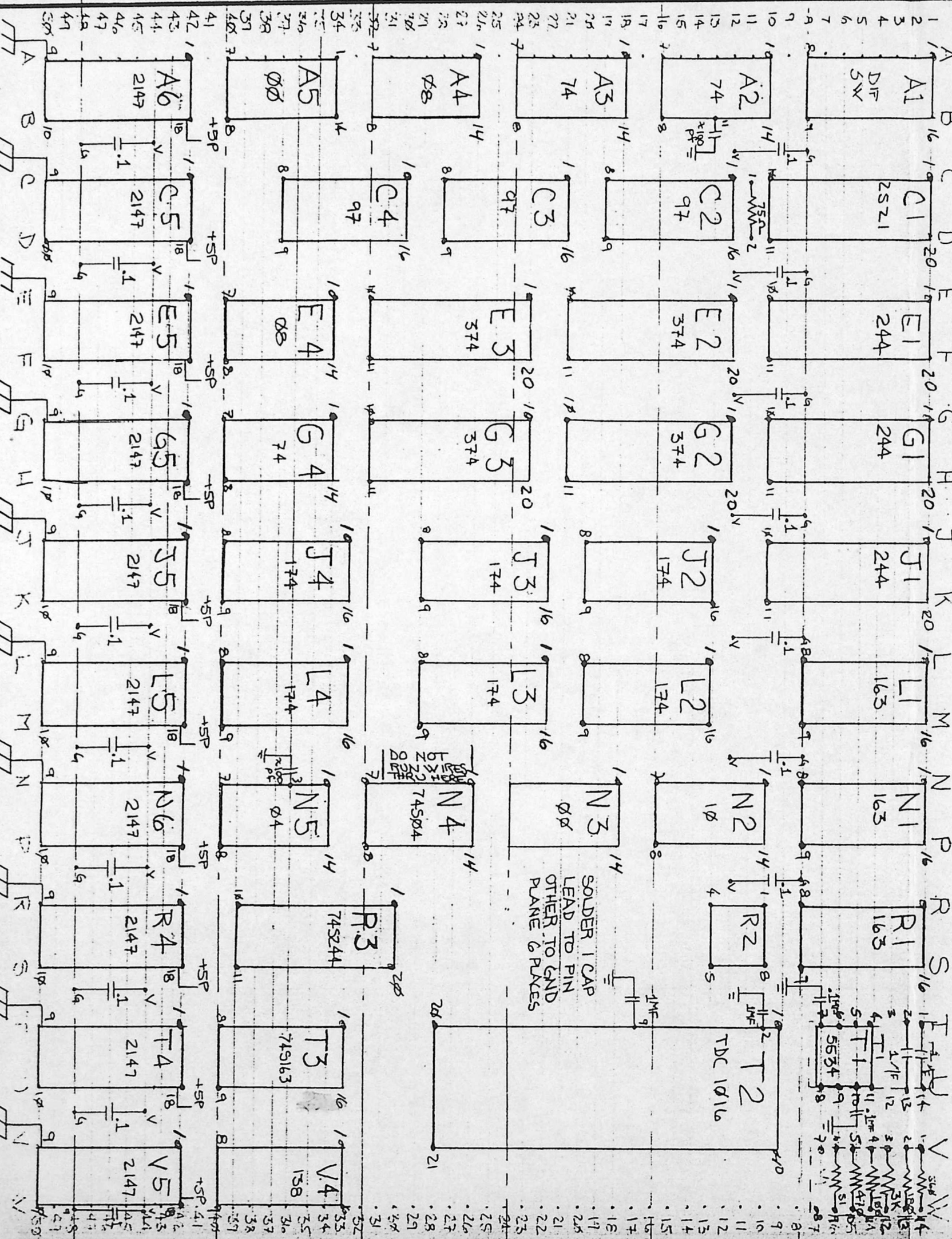
HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE
40	100 VERT BLKG START	BIN		10			
41	101 VERT BLKG WIDTH	BIN		10			
42	102 MISC 1 (SEC OV, EX3, SB, VIDEO SEL)			6			
43	103 OVERLAP (FRAME)			1			
100	400 CONTROL 1 (RATES, 3D)			3			
48	110 H POSITION CFG AMP	OFF	MD	12	+10	HF	CIC-1-1
49	111 V POSITION	↓	↓	↓	↓	↓	↓
4A	112 WIDTH	↓	↓	↓	↓	↓	↓
4B	113 DEPTH	↓	↓	↓	↓	↓	↓
50	120 WIDTH	OFF	D	12	+10	LF	CIC-1-2
51	121 D PAR	↓	↓	↓	↓	↓	↓
52	122 H PAR	↓	↓	↓	↓	↓	↓
53	123 L PAR	↓	↓	↓	↓	↓	↓
58	130 I PAR	OFF	MD	12	+10	HF	CIC-1-1
59	131 J PAR	↓	↓	↓	↓	↓	↓
5A	132 K PAR	↓	↓	↓	↓	↓	↓
5B	133 DEPTH	↓	D	↓	↓	↓	↓
60	140 A PAR	OFF	MD	12	+10	HF	CIC-1-1
61	141 B PAR	↓	↓	↓	↓	↓	↓
62	142 E PAR	↓	↓	↓	↓	↓	↓
63	143 F PAR	↓	↓	↓	↓	↓	↓
68	150 C PAR	OFF	MD	12	+10	HF	CIC-1-1
69	151 G PAR	↓	↓	↓	↓	↓	↓
6A	152 H BLKG START CFG	↓	↓	↓	↓	↓	↓
6B	153 H BLKG WIDTH CFG	↓	↓	↓	↓	↓	↓

RPU NEST 2

HEX	OCT	CODE	DAC	BITS	VOUT	FREQ	TYPE					
70	160 SPARE	BIN	MD	11	<u>+10</u>	HF	CIC-1-3					
71	161 VERT CTR		MD									
72	162 H BLKG START		D									
73	163 H BLKG WIDTH		D									
78	170 MASK 1 RAD	OFF	D	12	<u>+10</u>	LF	CIC-1-2					
79	171 MASK 2 RAD											
7A	172 MASK 3 RAD											
7B	173 HEIGHT											
80	200 MASK 2 SIN	ODD	MD	!@	<u>+10</u>	HF	CIC-1-1					
81	201 MASK 2 COS											
82	202 MASK 3 SIN											
83	203 MASK 3 COS											
88	210	SPARE										
8F	217											

PCB	CIRC	
5	20	CIC-1-1
2	8	CIC-1-2
1	3	CIC-1-3
8		

45P-WRAP 26 GAUGE WIRE TO PIN 18 FEED THRU HOLE IN ROW 41 & SOLDER DIRECTLY TO VOLTAGE PLANE
77-WRAP 26 GAUGE WIRE TO PIN 9 & SOLDER OTHER END DIRECTLY TO GND PLANE



DESIGNATION	QNTY	PART #	MANUFACTURER	REMARKS
A1	1	16 PIN DIP SW	CTS	NOT GRAYHILL XIF4
A2, A3, G4	3	74874		TTL
A4, E4	2	74508		TTL
A5, C5, E5, G5, J5, L5, N6, R4, T4, V4	10	2147H-2	INTEL	4K x1 STATIC RAM 45nsec
C2, C3, C4	3	7497		TTL
E1, G1, J1, E2, G2, E3, G3	3	74LS244		TTL
J2, L2, J3, L3, J4, L4	4	74LS374		TTL
L1, N1, R1, N2	6	74LS174		TTL
N3, A5	3	74LS163		TTL
N4	1	74LS10		TTL
N5	2	74S00		TTL
V4	1	74LS04		TTL
T1	1	74LS138		TTL
	1	NE5534N	SIGNETICS	OP AMP
	19			.1 MF CAPS
	4			1 MF CAPS
R2	1	7102B-210-101	BOURNS	DUAL 100K VARIABLE RES.
T2	1	TDC1016J-8	TRW	DIGITAL/ANALOG CONVR
V1-1	1			500Ω 1/4 WATT RES
V1-2	1			100Ω 1/4 WATT RES
V1-3	1			3KΩ 1/4 WATT RES
V1-4	1			100Ω 1/4 WATT RES
V1-5	1			470Ω 1/4 WATT RES
V1-6	1			51Ω 1/4 WATT RES
C1	1	25LS2521	AMS	14 PIN HEADER
N1	1			2 AMP PICO FUSLS
R3	1	74S244		TTL
T3	1	74S163		TTL
N4	1	74S04		TTL
A2-11, N5-3	2			100pf CAPS

ATA CORP.

COMPUTER IMAGE

FUNCTION GENERATOR

Board Layout

DATE	7-14-81
REV A	8/19/81
SIZE	B
DRAWING NO.	010713L1
DID NOT SCALE DRAWING	
SHEET	

~~*INSTRUCTIONS AND NOTES FOR PREPARATION AND WIREWRAP OF THE
COMPUTER IMAGE FUNCTION GENERATOR*~~

PREPARATION FOR WIREWRAPPING

1. REMOVE PINS ACCORDING TO ASSEMBLERS LAYOUT SHEET
2. CUT GROUND PLANE ACCORDING TO ASSEMBLERS LAYOUT FIG. 1
3. WITH KROY LABELING SYSTEM LABEL ALL LOCATIONS ACCORDING TO ASSEMBLERS LAYOUT
4. SOLDER 18 GAUGE BUSWIRE FROM PIN *Z0-62 TO *Z0-63 TO DIGITAL GROUNDPLANE AND FROM PIN *Z0-122 TO *Z0-123 TO DIGITAL GROUNDPLANE

** YOU ARE NOW READY TO GO TO WIREWRAP LIST. GOOD LUCK AND HAPPY WIRING **
**
** REFER TO ALL SOLDER AND WIRING NOTES WHILE FOLLOWING WIREWRAP LIST **

SD.1-1 SOLDER .1 uf CAPACITORS TO PINS ON WIREWRAPLIST. DISREGARD THE X IN FRONT OF PIN POSITIONS. SOLDER OTHER LEG OF CAPACITORS DIRECTLY TO THE DIGITAL GROUNDPLANE.

SD.1-2 CAPS1 ARE .1 uf CAPACITORS. ONE LEG IS SOLDERED TO THE PIN LISTED THE OTHER LEG IS SOLDERED DIRECTLY TO THE ISOLATED GROUNDPLANE. CAPS2 ARE 1mf CAPACITORS. ONE LEG IS SOLDERED TO THE PIN LISTED. THE OTHER LEG IS SOLDERED DIRECTLY TO THE ISOLATED GROUNDPLANE.

SD.1-3 CAP3 AND CAP4 ARE 1 uf CAPACITORS. CAP3 IS SOLDERED WITH ONE LEG T.2-2 AND THE OTHER TO T.2-3 CAP4 IS SOLDERED WITH ONE LEG TO T.2-9 AND THE OTHER LEG TO T.2-10

SD.2-1 WITH A SIX INCH LENGTH OF 26 GAUGE WIRE, STRIP INSULATION FROM WIRE AND WRAP TO PINS LISTED. INSERT OTHER END OF WIRE THRU NEAREST HOLE IN BOARD AND SOLDER DIRECTLY TO VOLTAGE PLANE (VCC).

SD.2-2 WITH A SIX INCH LENGTH OF 26 GAUGE WIRE, STRIP WIRE AND WRAP ONE END OF WIRE TO PINS LISTED AND SOLDER OTHER END DIRECTLY TO THE DIGITAL GROUNDPLANE.

SD.2-3 WITH 18 GAUGE BUSWIRE SOLDER TO BUS PIN *Z0-57 SLEEVE WIRE AND SOLDER OTHER END DIRECTLY TO ISOLATED GROUNDPLANE

PP.1-1 ALL WIRES MUST BE WRAPPED DIRECTLY TO A GROUND PIN

PP.1-2 ALL WIRES MUST BE WRAPPED DIRECTLY TO A VOLTAGE PIN

PP.1-3 ALL WIRES MUST BE WRAPPED TO THE ISOLATED GROUND PINS

PP.1-4 GROUND WIRE OF TWISTED PAIR MUST USE ISOLATED GROUND

TWIST STANDS FOR TWISTED PAIR. WIRE WRAP ONE END OF YELLOW WIRE TO CLOSEST GROUND PIN. WRAP ONE END OF BLUE WIRE TO PIN LISTED. TWIST WIRES TOGETHER AND WRAP BLUE WIRE TO NEXT PIN LISTED. WRAP REMAINING WIRE TO GROUND PIN. FOLLOW TWISTED PAIR ROUTING DIAGRAMS.

ROUTE REFERS TO A ROUTING DIAGRAM

***** IMPORTANT *****
***** DO NOT DEVIATE FROM WIREWRAP LIST AND ROUTING DIAGRAMS *****

NOTE SD.1-1

CAPS	XA.1-20	XC.1-20	XE.1-20	XR.1-20	XA.5-18	XC.5-18	XE.5-18
	XG.6-18	XJ.6-18	XL.5-18	XN.5-18	XR.5-18	XT.3-18	XV.3-18

NOTE SD.1-2

CAPS1 XT.1-4 XT.1-7

CAPS2 XT.2-2 XT.2-4

NOTE SD.1-3

CAP3 XT.2-2 XT.2-3

CAP4 XT.2-9 XT.2-10

NOTE SD.2-1

+5P	A.4-16	A.5-18	C.5-18	E.4-16	E.5-18	G.6-18	J.6-18
	L.5-18	N.5-18	T.3-18	V.3-18			

NOTE SD.2-2

-GNDP	A.4-8	A.5-9	C.4-8	C.5-9	E.4-8	E.5-9	G.6-9
	J.6-9	L.5-9	N.5-9	R.5-9	T.3-9	V.3-9	R.1-10

NOTE SD.2-3

-GNDI *Z0-57

TWIST FG.1-1

BMCLK J.1-4 J.1-5 J.4-1

TWIST FG.1-2

BMCLK/	J.1-2	J.1-3	J.2-3	J.2-11	G.3-3	L.2-9	L.3-9
	L.4-9						

TWIST FG.1-3

BMCLKD/ J.1-6 J.5-2 E.4-2 C.4-2 A.4-2

TWIST FG.1-4

MCLK J.1-1 *Z0-87

NOTE PP.1-1

TWIST FG.1-5

AOUT T.1-3 T.2-7

TWIST FG.1-6

*FUNCTION GENERATOR

*11/16/81

PAGE

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FSYNCH/	R.2-5 J.3-5	R.2-12 G.3-6	R.2-2 J.5-1	J.2-13	J.2-1	J.3-1	J.3-10
TWIST	FG.1-7						
HSYNCH/	G.1-13	*Z0-5					
TWIST	FG.1-8						
SSYNCH/	G.1-1	*Z0-6					
END	X.X-1						
NOTE	PP.1-2						
-GNDP	A.1-10 E.2-8 J.1-7 L.4-8 R.4-10	A.2-10 E.3-8 J.2-7 N.1-8 T.2-10	A.3-8 G.1-7 J.3-7 N.2-8	C.1-10 G.2-7 J.4-7 N.3-10	C.2-8 G.3-7 J.5-8 N.4-10	C.3-8 G.4-7 L.2-8 R.2-7	E.1-10 G.5-7 L.3-8 R.3-10
END	X.X-2						
-GND	A.1-1 C.1-1 L.1-13 R.1-19	A.1-19 E.1-19 L.1-14 R.1-1	A.2-1 E.1-1 L.1-15 R.3-1	A.2-16 J.2-2 L.2-10 R.4-1	A.2-18 L.1-10 L.2-11 T.2-17	A.3-5 L.1-11 N.3-1	C.1-19 L.1-12 N.4-1
NOTE	PP.1-3						
-GNDI	T.2-5	T.2-6	T.2-8	V.2-2	V.2-6		
NOTE	PP.1-4						
+5P	A.1-20 E.2-16 J.1-14 L.4-16 R.3-20	A.2-20 E.3-16 J.2-14 N.1-16 R.4-20	A.3-16 G.1-14 J.3-14 N.2-16 T.2-9	C.1-20 G.2-14 J.4-14 N.3-20	C.2-16 G.3-14 J.5-16 N.4-20	C.3-16 G.4-14 L.2-16 R.1-20	E.1-20 G.5-14 L.3-16 R.2-14
END	X.X-3						
+5	A.4-6 E.4-6 G.3-11 J.5-7	A.4-1 E.4-1 G.3-4 L.4-1	C.2-1 G.2-4 G.3-1 L.4-4	C.3-1 G.2-2 J.5-6 L.4-14	C.4-1 G.2-10 J.5-4 N.1-1	E.2-1 G.2-12 J.5-3 N.2-1	E.3-1 G.3-12 J.5-5
+15	T.1-7	*Z0-53					
-15	T.1-4	*Z0-55					
-5	T.2-2	V.2-1	V.2-10	*Z0-64			
ROUTE	FG.2-1						
RPUA0	C.1-2	*Z0-70					

RPUA1	A.1-2	*Z0-71
RPUA2	A.1-4	*Z0-72
RPUA3	A.1-6	*Z0-73
RPUA4	A.1-8	*Z0-74
RPUA5	A.1-11	*Z0-75
RPUA6	A.1-13	*Z0-76
RPUA7	A.1-15	*Z0-77
RPUA8	A.1-17	*Z0-78

ROUTE FG.2-2

BA0	A.3-1	C.1-18
BA1	A.1-18	A.3-2
BA2	A.1-16	A.2-13
BA3	A.1-14	A.2-11
BA4	A.1-12	A.2-8
BA5	A.1-9	A.2-6
BA6	A.1-7	A.2-4
BA7	A.1-5	A.2-2
BA8	A.1-3	A.3-3

ROUTE FG.2-3

FA0	G.4-9 L.5-1	E.4-14 N.5-1	A.5-1 R.5-1	C.5-1 T.3-1	E.5-1 V.3-1	G.6-1	J.6-1
FA1	G.4-10 L.5-2	E.4-13 N.5-2	A.5-2 R.5-2	C.5-2 T.3-2	E.5-2 V.3-2	G.6-2	J.6-2
FA2	G.4-11 L.5-3	E.4-12 N.5-3	A.5-3 R.5-3	C.5-3 T.3-3	E.5-3 V.3-3	G.6-3	J.6-3
FA3	C.4-14 N.5-4	A.5-4 R.5-4	C.5-4 T.3-4	E.5-4 V.3-4	G.6-4	J.6-4	L.5-4
FA4	C.4-13 N.5-5	A.5-5 R.5-5	C.5-5 T.3-5	E.5-5 V.3-5	G.6-5	J.6-5	L.5-5
FA5	C.4-12 N.5-6	A.5-6 R.5-6	C.5-6 T.3-6	E.5-6 V.3-6	G.6-6	J.6-6	L.5-6
FA6	C.4-11	A.5-17	C.5-17	E.5-17	G.6-17	J.6-17	L.5-17

FA6	N.5-17	R.5-17	T.3-17	V.3-17			
FA7	A.4-14 N.5-16	A.5-16 R.5-16	C.5-16 T.3-16	E.5-16 V.3-16	G.6-16	J.6-16	L.5-16
FA8	A.4-13 N.5-15	A.5-15 R.5-15	C.5-15 T.3-15	E.5-15 V.3-15	G.6-15	J.6-15	L.5-15
FA9	A.4-12 N.5-14	A.5-14 R.5-14	C.5-14 T.3-14	E.5-14 V.3-14	G.6-14	J.6-14	L.5-14

ROUTE FG.2-4

RPUD0 E.1-2 *Z0-10

RPUD1 E.1-4 *Z0-11

RPUD10 C.1-8 *Z0-20

RPUD11 C.1-11 *Z0-21

RPUD12 C.1-13 *Z0-22

RPUD13 C.1-15 *Z0-23

RPUD14 C.1-17 *Z0-24

RPUD2 E.1-6 *Z0-12

RPUD3 E.1-8 *Z0-13

RPUD4 E.1-11 *Z0-14

RPUD5 E.1-13 *Z0-15

RPUD6 E.1-15 *Z0-16

RPUD7 E.1-17 *Z0-17

RPUD8 C.1-4 *Z0-18

RPUD9 C.1-6 *Z0-19

ROUTE FG.2-5

BD0 A.5-11 N.4-3 N.1-3 E.1-18 E.2-6

BD1 C.5-11 N.4-4 N.1-4 E.1-16 E.2-11

BD10 C.1-12 N.1-14 N.3-8

BD11 C.1-9 N.3-13

BD12 C.1-7 N.3-14

BD13 C.1-5 N.3-17

BD14	C.1-3	N.3-18			
BD2	E.5-11	N.4-7	N.1-6	E.1-14	E.2-13
BD3	G.6-11	N.4-8	E.1-12	E.2-14	
BD4	J.6-11	N.4-13	C.2-3	E.1-9	
BD5	L.5-11	N.4-14	E.1-7	C.2-4	
BD6	N.5-11	N.4-17	E.1-5	C.2-6	
BD7	R.5-11	N.3-3	E.1-3	C.2-11	
BD8	T.3-11	N.3-4	N.1-11	C.1-16	C.2-13
BD9	V.3-11	N.3-7	N.1-13	C.1-14	C.2-14

ROUTE FG.2-6

FD0	A.5-7	T.2-37	
FD1	C.5-7	T.2-35	
FD2	E.5-7	T.2-33	R.1-2
FD3	G.6-7	T.2-31	R.1-4
FD4	J.6-7	T.2-29	R.1-6
FD5	L.5-7	T.2-27	R.1-8
FD6	N.5-7	T.2-25	R.1-11
FD7	R.5-7	T.2-23	R.1-13
FD8	T.2-19	T.3-7	R.1-15
FD9	T.2-16	V.3-7	R.1-17

ROUTE FG.2-7

LFD2	R.1-18	*Z0-97
LFD3	R.1-16	*Z0-96
LFD4	R.1-14	*Z0-95
LFD5	R.1-12	*Z0-94
LFD6	R.1-9	*Z0-93
LFD7	R.1-7	*Z0-92
LFD8	R.1-5	*Z0-91
LFD9	R.1-3	*Z0-90

END X.X-4

LD RAM/	J.4-9 J.6-8	G.3-10 L.5-8	A.3-11 N.5-8	A.5-8 R.5-8	C.5-8 T.3-8	E.5-8 V.3-8	G.6-8
PEN/	J.2-8 N.5-10	A.5-10 R.5-10	C.5-10 T.3-10	E.5-10 V.3-10	G.6-10	J.6-10	L.5-10
SWAV0	N.2-2 N.5-13	A.5-13 R.5-13	C.5-13 T.3-13	E.5-13 V.3-13	G.6-13	J.6-13	L.5-13
SWAV1	N.2-5 N.5-12	A.5-12 R.5-12	C.5-12 T.3-12	E.5-12 V.3-12	G.6-12	J.6-12	L.5-12
A.2-12	A.2-12	L.1-3					
A.2-14	A.2-14	L.1-2					
A.2-19	A.2-19	G.1-9					
A.2-3	A.2-3	L.1-7					
A.2-5	A.2-5	L.1-6					
A.2-7	A.2-7	L.1-5					
A.2-9	A.2-9	L.1-4					
BHSYNCH	G.1-12	G.1-11					
BSSYNCH	G.1-2	G.1-3	R.3-11	R.4-11			
BHSYNCH/	G.1-10	G.2-11					
BSSYNCH/	G.1-4	G.2-3	G.5-5	J.4-10			
C.2-10	C.2-10	C.3-11					
C.2-12	C.2-12	C.3-13					
C.2-15	C.2-15	C.3-14					
C.2-2	C.2-2	C.3-3					
C.2-5	C.2-5	C.3-4					
C.2-7	C.2-7	C.3-6					
C.3-10	A.4-3	C.3-10					
C.3-12	A.4-4	C.3-12					
C.3-15	A.4-5	C.3-15					
C.3-2	C.3-2	C.4-4					
C.3-5	C.3-5	C.4-5					

C.3-7	C.3-7	C.4-6		
C.4-15	A.4-10	C.4-15		
E.2-10	E.2-10	E.3-11		
E.2-12	E.2-12	E.3-13		
E.2-15	E.2-15	E.3-14		
E.2-7	E.2-7	E.3-6		
E.3-10	E.3-10	E.4-4		
E.3-12	E.3-12	E.4-5		
E.3-15	C.4-3	E.3-15		
E.3-7	E.3-7	E.4-3		
FCLK/	R.2-1	R.2-4	R.2-13	J.4-3
FSYNCH	G.3-5	L.2-13	L.3-13	L.4-13
G.1-6	G.1-6	J.3-4		
G.1-8	A.3-6	G.1-8		
G.2-6	G.2-6	J.4-4		
G.2-8	G.2-8	J.4-5		
G.4-8	G.4-8	G.5-10		
G.5-3	G.5-3	G.5-4		
G.5-8	C.4-10	G.5-8		
ICLK	G.4-6	J.3-12	J.5-10	
IEN	J.3-13	J.5-15		
J.1-8	J.1-8	J.2-4		
J.2-5	J.2-5	J.2-12		
J.3-11	J.1-9	J.3-11		
J.3-3	G.2-13	J.3-3		
J.3-6	G.2-1	J.3-6		
J.3-8	A.4-9	C.4-9	E.4-9	J.3-8
J.4-6	G.3-2	J.4-6		
L.2-12	G.4-3	L.2-12	L.2-5	

L.3-10	L.2-7	L.3-10	L.3-11	
L.3-12	G.4-5	L.3-12	L.4-12	L.4-5
L.3-5	G.4-4	L.3-5		
L.3-7	L.3-7	L.4-10	L.4-11	
LCNTROL/	A.3-13	G.3-13	N.1-9	
LDAC/	R.2-11	R.2-6	*20-98	
LFREQ/	A.3-15	N.3-11	N.4-11	
LOADM	G.3-9	G.5-2		
LOADM/	G.3-8	J.2-10	J.3-9	
LPHASE	G.5-1	J.1-12		
LPHASE/	A.3-14	C.2-9	E.2-9	J.1-13
N.1-10	N.1-10	N.2-11		
N.1-12	N.1-12	N.2-13		
N.1-15	N.1-15	N.2-14		
N.1-2	N.1-2	N.2-3		
N.1-5	N.1-5	N.2-4		
N.1-7	N.1-7	N.2-6		
N.3-12	N.3-12	R.3-13		
N.3-15	N.3-15	R.3-14		
N.3-16	N.3-16	R.3-17		
N.3-19	N.3-19	R.3-18		
N.3-2	N.3-2	R.3-3		
N.3-5	N.3-5	R.3-4		
N.3-6	N.3-6	R.3-7		
N.3-9	N.3-9	R.3-8		
N.4-12	N.4-12	R.4-13		
N.4-15	N.4-15	R.4-14		
N.4-16	N.4-16	R.4-17		
N.4-2	N.4-2	R.4-3		

N.4-5	N.4-5	R.4-4			
N.4-6	N.4-6	R.4-7			
N.4-9	N.4-9	R.4-8			
PEN	A.4-7	C.4-7	E.4-7	J.2-9	J.4-2
PSYNCH	C.3-9	E.3-9	G.5-6		
R.3-12	L.2-14	R.3-12			
R.3-15	L.2-15	R.3-15			
R.3-16	L.2-2	R.3-16			
R.3-19	L.2-3	R.3-19			
R.3-2	L.3-2	R.3-2			
R.3-5	L.3-3	R.3-5			
R.3-6	L.2-4	R.3-6			
R.3-9	L.2-1	R.3-9			
R.4-12	L.3-1	R.4-12			
R.4-15	L.3-14	R.4-15			
R.4-16	L.3-15	R.4-16			
R.4-2	L.4-15	R.4-2			
R.4-5	L.4-2	R.4-5			
R.4-6	L.4-3	R.4-6			
R.4-9	L.3-4	R.4-9			
RPUIOSL/	A.2-15	*Z0-69			
RPUSTRB/	A.2-17	*Z0-3			
RPUWRT/	A.3-4	*Z0-4			
RSSYNCH	J.4-8	N.2-9			
SSPEED0	J.1-11	N.2-10			
SSPEED0/	E.4-10	G.5-9	J.1-10		
SSPEED1	J.5-9	N.2-12			
SYNSEL	G.1-5	J.3-2	N.2-15		
T.2-12	R.2-3	T.2-12			

T.2-4	T.2-4	V.1-8	
V.1-5	V.1-5	V.2-9	
V.1-7	V.1-7	V.2-13	
V.2-11	T.1-2	V.2-11	V.2-12
V.2-14	V.1-2	V.2-14	
V.2-4	V.1-6	V.2-4	
V.2-5	V.1-4	V.2-5	
VOUT	T.1-6	V.2-3	*20-51

TOTAL NUMBER OF WIRE WRAPS: 1154

TOTAL PINS USED: 828

15	T.1-10	*Z0-53					
+5	A.3-4 G.4-12 L.1-6 R.1-1	A.3-2 G.4-11 L.1-1 T.3-6	A.3-10 G.4-4 L.2-1 T.3-4	A.3-12 G.4-1 L.3-1 T.3-3	C.2-1 J.2-1 L.4-1 T.3-5	C.2-4 J.3-1 N.1-1 T.3-7	C.2-14 J.4-1 R.1-6
+5P	A.2-14 C.3-16 E.5-18 J.2-16 L.4-16 N.6-18 V.4-16	A.3-14 C.4-16 G.1-20 J.3-16 L.5-18 R.1-16 V.5-18	A.4-14 C.5-18 G.2-20 J.4-16 N.1-16 R.3-20	A.5-14 E.1-20 G.3-20 J.5-18 N.2-14 R.4-18	A.6-18 E.2-20 G.4-14 L.1-16 N.3-14 T.2-9	C.1-20 E.3-20 G.5-18 L.2-16 N.4-14 T.3-16	C.2-16 E.4-14 J.1-20 L.3-16 N.5-14 T.4-18
-15	T.1-7	*Z0-55					
-5	T.1-14	T.2-2	V.1-1	V.1-10	*Z0-64		
-GND	A.1-10 C.1-1 E.2-1 J.1-1	A.1-11 C.1-16 E.3-1 R.3-19	A.1-12 C.1-18 G.1-19 R.3-1	A.1-13 C.4-10 G.1-1 T.2-17	A.1-14 C.4-11 G.2-1 V.4-5	A.1-15 E.1-19 G.3-1	A.2-2 E.1-1 J.1-19
-GNDI	T.1-13	T.2-5	T.2-6	T.2-8	V.1-2	V.1-6	*Z0-57
GNDP	A.2-7 C.3-8 E.5-9 J.2-8 L.4-8 N.6-9 V.4-8	A.3-7 C.4-8 G.1-10 J.3-8 L.5-9 R.1-8 V.5-9	A.4-7 C.5-9 G.2-10 J.4-8 N.1-8 R.3-10	A.5-7 E.1-10 G.3-10 J.5-9 N.2-7 R.4-9	A.6-9 E.2-10 G.4-7 L.1-8 N.3-7 T.2-10	C.1-10 E.3-10 G.5-9 L.2-8 N.4-7 T.3-8	C.2-8 E.4-7 J.1-10 L.3-8 N.5-7 T.4-9
BMCLK	N.3-9	N.4-4	N.4-5				
BMCLK/	A.2-3 N.4-2	A.2-11	C.2-9	C.3-9	C.4-9	G.4-3	N.4-3
BMCLKD/	L.1-2	N.1-2	N.4-6	R.1-2	T.3-2		
MCLK	N.4-1	*Z0-87					
A.2-5	A.2-5	A.2-12					
A.3-6	A.3-6	N.3-4					
A.3-8	A.3-8	N.3-5					
A.5-3	A.5-3	A.5-4					
A0	G.1-3	V.4-1					
BA1	J.1-18	V.4-2					
BA2	C.1-13	J.1-16					

BA3	C.1-11	J.1-14			
BA4	C.1-8	J.1-12			
BA5	C.1-6	J.1-9			
BA6	C.1-4	J.1-7			
BA7	C.1-2	J.1-5			
BA8	J.1-3	V.4-3			
BD0	A.6-11	E.1-18	E.2-3	J.4-3	L.2-6
BD1	C.5-11	E.1-16	E.2-4	J.4-4	L.2-11
BD10	G.1-14	G.2-8	J.4-14		
BD11	G.1-12	G.2-13			
BD12	G.1-9	G.2-14			
BD13	G.1-7	G.2-17			
BD14	G.1-5	G.2-18			
BD2	E.1-14	E.2-7	E.5-11	J.4-6	L.2-13
BD3	E.1-12	E.2-8	G.5-11	L.2-14	
BD4	E.1-9	E.2-13	J.2-3	J.5-11	
BD5	E.1-7	E.2-14	J.2-4	L.5-11	
BD6	E.1-5	E.2-17	J.2-6	N.6-11	
BD7	E.1-3	G.2-3	J.2-11	R.4-11	
BD8	G.1-18	G.2-4	J.2-13	J.4-11	T.4-11
BD9	G.1-16	G.2-7	J.2-14	J.4-13	V.5-11
BHSYNCH	N.5-8	N.5-11			
BHSYNCH/	A.3-11	N.5-10			
BSSYNCH	E.3-11	G.3-11	N.5-4	N.5-5	
BSSYNCH/	A.3-3	A.5-5	N.3-1	N.5-6	
C.1-12	A.1-3	C.1-12			
C.1-14	A.1-2	C.1-14			
C.1-19	C.1-19	N.5-13			
C.1-3	A.1-7	C.1-3			

C.1-5	A.1-6	C.1-5					
●.1-7	A.1-5	C.1-7					
C.1-9	A.1-4	C.1-9					
C.3-10	C.3-10	C.3-11	C.4-7				
C.3-12	C.2-12	C.2-5	C.3-12	N.2-13			
C.3-5	C.3-5	N.2-2					
C.3-7	C.2-10	C.2-11	C.3-7				
C.4-12	C.4-12	C.4-5	N.2-1				
E.2-12	E.2-12	E.3-13					
E.2-15	E.2-15	E.3-14					
E.2-16	E.2-16	E.3-17					
E.2-2	E.2-2	E.3-3					
E.2-5	E.2-5	E.3-4					
E.2-6	E.2-6	E.3-7					
●.2-9	E.2-9	E.3-8					
E.3-12	C.3-1	E.3-12					
E.3-15	C.3-14	E.3-15					
E.3-16	C.3-15	E.3-16					
E.3-2	C.2-15	E.3-2					
E.3-5	C.2-2	E.3-5					
E.3-6	C.2-3	E.3-6					
E.3-9	C.3-4	E.3-9					
E.4-11	E.4-11	L.1-9	N.1-9	R.1-9			
E.4-3	A.3-13	E.4-3					
E.4-6	A.3-1	E.4-6					
E.4-8	E.4-8	N.4-9					
FA0	A.6-1 N.6-1	C.5-1 R.1-14	E.5-1 R.4-1	G.5-1 T.4-1	J.5-1 V.5-1	L.5-1	N.2-3
FA1	A.6-2 N.6-2	C.5-2 R.1-13	E.5-2 R.4-2	G.5-2 T.4-2	J.5-2 V.5-2	L.5-2	N.2-4

FA2	A.6-3 N.6-3	C.5-3 R.1-12	E.5-3 R.4-3	G.5-3 T.4-3	J.5-3 V.5-3	L.5-3	N.2-5
FA3	A.6-4 N.6-4	C.5-4 R.4-4	E.5-4 T.4-4	G.5-4 V.5-4	J.5-4	L.5-4	N.1-14
FA4	A.6-5 N.6-5	C.5-5 R.4-5	E.5-5 T.4-5	G.5-5 V.5-5	J.5-5	L.5-5	N.1-13
FA5	A.6-6 N.6-6	C.5-6 R.4-6	E.5-6 T.4-6	G.5-6 V.5-6	J.5-6	L.5-6	N.1-12
FA6	A.6-17 N.6-17	C.5-17 R.4-17	E.5-17 T.4-17	G.5-17 V.5-17	J.5-17	L.5-17	N.1-11
FA7	A.6-16 N.6-16	C.5-16 R.4-16	E.5-16 T.4-16	G.5-16 V.5-16	J.5-16	L.1-14	L.5-16
FA8	A.6-15 N.6-15	C.5-15 R.4-15	E.5-15 T.4-15	G.5-15 V.5-15	J.5-15	L.1-13	L.5-15
FA9	A.6-14 N.6-14	C.5-14 R.4-14	E.5-14 T.4-14	G.5-14 V.5-14	J.5-14	L.1-12	L.5-14
FCLK/	A.4-1	A.4-9	A.4-12	N.3-8			
FD0	A.6-7	T.2-37					
FD1	C.5-7	T.2-35					
FD2	E.5-7	R.3-2	T.2-33				
FD3	G.5-7	R.3-4	T.2-31				
FD4	J.5-7	R.3-6	T.2-29				
FD5	L.5-7	R.3-8	T.2-27				
FD6	N.6-7	R.3-11	T.2-25				
FD7	R.3-13	R.4-7	T.2-23				
FD8	R.3-15	T.2-19	T.4-7				
FD9	R.3-17	T.2-16	V.5-7				
FSYNCH	C.2-13	C.3-13	C.4-13	G.4-5			
FSYNCH/	A.2-1 E.4-5	A.2-13 G.4-6	A.4-2 T.3-1	A.4-10	A.4-13	E.4-13	E.4-1
G.2-12	G.2-12	G.3-13					
G.2-15	G.2-15	G.3-14					
G.2-16	G.2-16	G.3-17					

G.2-19	G.2-19	G.3-18	
●.2-2	G.2-2	G.3-3	
G.2-5	G.2-5	G.3-4	
G.2-6	G.2-6	G.3-7	
G.2-9	G.2-9	G.3-8	
G.3-12	C.4-14	G.3-12	
G.3-15	C.4-15	G.3-15	
G.3-16	C.4-2	G.3-16	
G.3-19	C.4-3	G.3-19	
G.3-2	C.3-2	G.3-2	
G.3-5	C.3-3	G.3-5	
G.3-6	C.4-4	G.3-6	
G.3-9	C.4-1	G.3-9	
HSYNCH/	N.5-9	*Z0-5	
●CLK	E.4-9	N.2-12	T.3-10
IEN	E.4-10	T.3-15	
J.2-10	J.2-10	J.3-11	
J.2-12	J.2-12	J.3-13	
J.2-15	J.2-15	J.3-14	
J.2-2	J.2-2	J.3-3	
J.2-5	J.2-5	J.3-4	
J.2-7	J.2-7	J.3-6	
J.3-10	J.3-10	L.1-3	
J.3-12	J.3-12	L.1-4	
J.3-15	J.3-15	L.1-5	
J.3-2	J.3-2	N.1-4	
J.3-5	J.3-5	N.1-5	
●J.3-7	J.3-7	N.1-6	
J.4-10	J.4-10	L.4-11	

J.4-12	J.4-12	L.4-13					
●.4-15	J.4-15	L.4-14					
J.4-2	J.4-2	L.4-3					
J.4-5	J.4-5	L.4-4					
J.4-7	J.4-7	L.4-6					
L.2-10	L.2-10	L.3-11					
L.2-12	L.2-12	L.3-13					
L.2-15	L.2-15	L.3-14					
L.2-7	L.2-7	L.3-6					
L.3-10	L.3-10	R.1-4					
L.3-12	L.3-12	R.1-5					
L.3-15	L.3-15	N.1-3					
L.3-7	L.3-7	R.1-3					
LCNTR0L/	G.4-13	J.4-9	V.4-13				
●LDAC/	A.4-8	A.4-11	*Z0-98				
LDRAM/	A.6-8 N.3-2	C.5-8 N.6-8	E.5-8 R.4-8	G.4-10 T.4-8	G.5-8 V.4-11	J.5-8 V.5-8	L.5-8
LFD2	R.3-18	*Z0-97					
LFD3	R.3-16	*Z0-96					
LFD4	R.3-14	*Z0-95					
LFD5	R.3-12	*Z0-94					
LFD6	R.3-9	*Z0-93					
LFD7	R.3-7	*Z0-92					
LFD8	R.3-5	*Z0-91					
LFD9	R.3-3	*Z0-90					
LFREQ/	E.2-11	G.2-11	V.4-15				
LOADM	A.5-2	G.4-9					
●LOADM/	A.2-10	E.4-12	G.4-8				
LPHASE	A.5-1	N.4-12					

LPHASE/	J.2-9	L.2-9	N.4-13	V.4-14			
●.1-15	L.1-10	N.1-15					
N.2-6	N.2-6	N.3-13					
N.3-11	N.1-10	N.3-11					
N.3-6	G.4-2	N.3-6					
N.4-8	A.2-4	N.4-8					
N.5-12	N.5-12	V.4-6					
N.5-2	E.4-4	N.5-2					
PEN	A.2-9	L.1-7	N.1-7	N.3-10	R.1-7		
PEN/	A.2-8 N.6-10	A.6-10 R.4-10	C.5-10 T.4-10	E.5-10 V.5-10	G.5-10	J.5-10	L.5-10
PSYNCH	A.5-6	J.3-9	L.3-9				
R.2-5	R.2-5	V.1-9					
R.2-7	R.2-7	V.1-13					
●RPUA0	G.1-17	*Z0-70					
RPUA1	J.1-2	*Z0-71					
RPUA2	J.1-4	*Z0-72					
RPUA3	J.1-6	*Z0-73					
RPUA4	J.1-8	*Z0-74					
RPUA5	J.1-11	*Z0-75					
RPUA6	J.1-13	*Z0-76					
RPUA7	J.1-15	*Z0-77					
RPUA8	J.1-17	*Z0-78					
RPUD0	E.1-2	*Z0-10					
RPUD1	E.1-4	*Z0-11					
RPUD10	G.1-6	*Z0-20					
RPUD11	G.1-8	*Z0-21					
●RPUD12	G.1-11	*Z0-22					
RPUD13	G.1-13	*Z0-23					

RPUD14	G.1-15	*Z0-24					
RPUD2	E.1-6	*Z0-12					
RPUD3	E.1-8	*Z0-13					
RPUD4	E.1-11	*Z0-14					
RPUD5	E.1-13	*Z0-15					
RPUD6	E.1-15	*Z0-16					
RPUD7	E.1-17	*Z0-17					
RPUD8	G.1-2	*Z0-18					
RPUD9	G.1-4	*Z0-19					
RPUIOSL/	C.1-15	*Z0-69					
RPUSTRB/	C.1-17	*Z0-3					
RPUWRT/	V.4-4	*Z0-4					
RSSYNCH	L.4-9	N.3-3					
SSPEED0	L.4-10	N.4-11					
SSPEED0/	N.3-12	N.4-10	R.1-10				
SSPEED1	L.4-12	T.3-9					
SSYNCH/	N.5-3	*Z0-6					
SWAV0	A.6-13 N.6-13	C.5-13 R.4-13	E.5-13 T.4-13	G.5-13 V.5-13	J.5-13	L.4-2	L.5-13
SWAV1	A.6-12 N.6-12	C.5-12 R.4-12	E.5-12 T.4-12	G.5-12 V.5-12	J.5-12	L.4-5	L.5-12
SYNSEL	E.4-2	L.4-15	N.5-1				
T.1-1	T.1-1	T.2-3					
T.2-12	A.4-3	T.2-12					
T.2-4	R.2-8	T.1-2	T.2-4				
T.2-7	T.1-6	T.2-7					
V.1-11	T.1-5	V.1-11	V.1-12				
V.1-14	R.2-2	V.1-14					
V.1-4	R.2-6	V.1-4					
V.1-5	R.2-4	V.1-5					

*LUXEBURG FG

*11/11/81

PAGE

9

VOUT

T.1-9

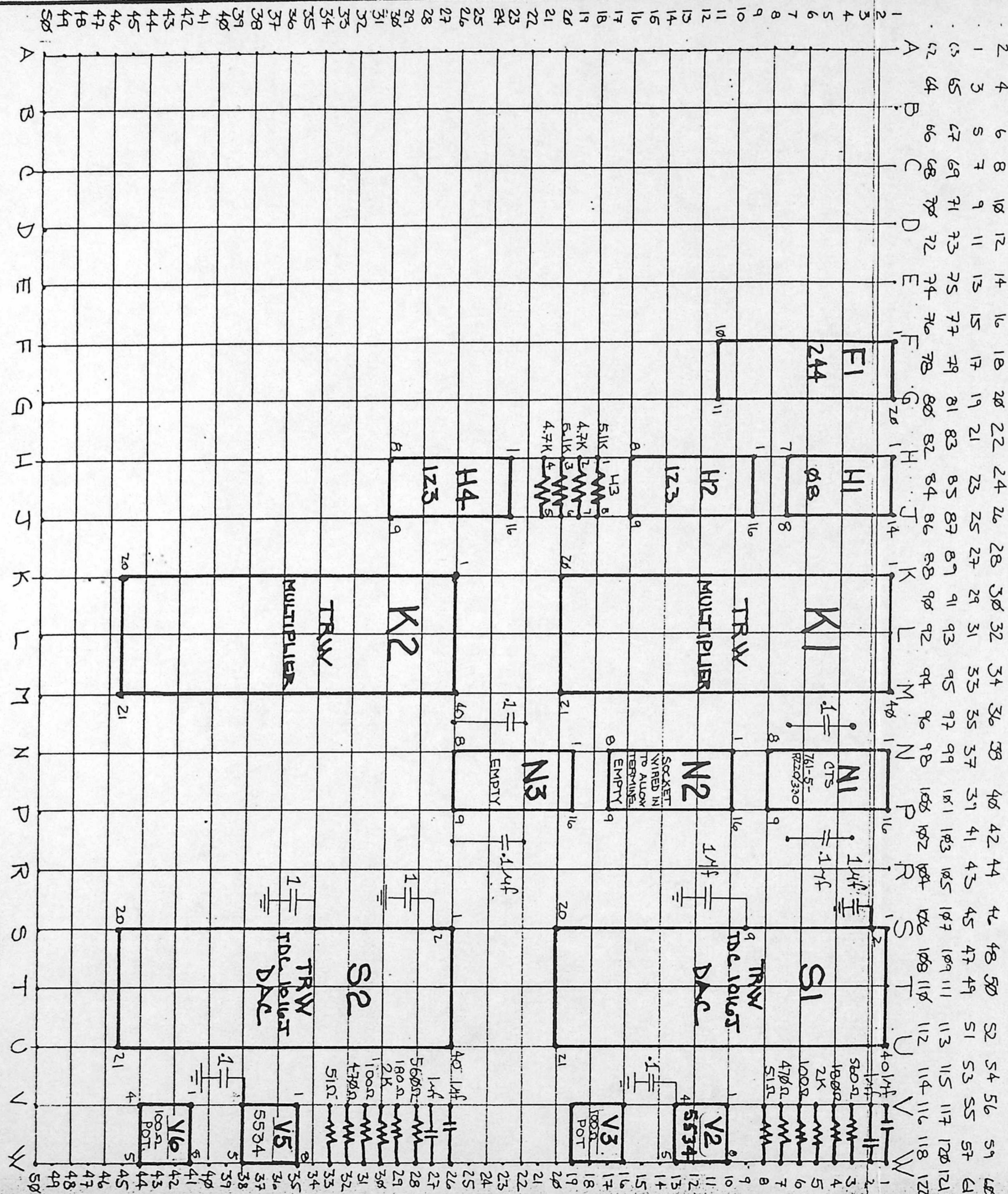
V.1-3

*Z0-51

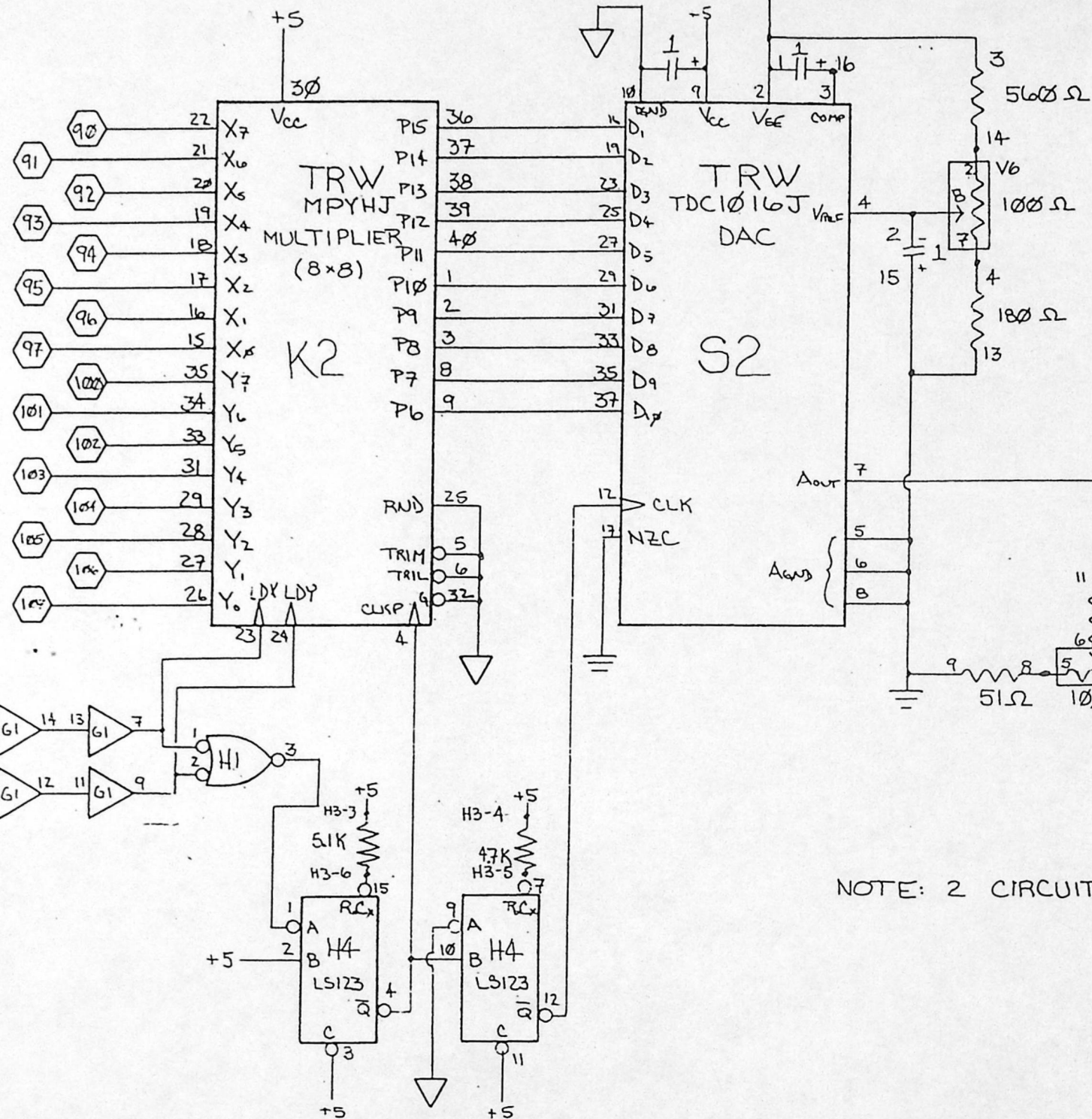
REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

DESIGNATION	QNTY	PART #	MFG	REMARKS
H1	1	74LS08		TTL
F1	1	74LS244		TTL
H2,H4	2	74LS123		TTL
K1,K2	2	MPY-8HJ	TRW	Op Amp
V2,V5	2	NE5534N	Signetics	Dual Dip 100ΩPots
V3,V6	2	7102B-210-101	Bourn	Dac
S1,S2	2	TDC1016J-8	TRW	1/4 Watt 4.7KΩRes.
H3-2&4	2			1/4 Watt 5.1KΩRes.
H3-1&3	2			1 uF Caps
V1,V4-1&2	8			560ΩRes 1/4 Watt
V1,V4-3	2			180ΩRes 1/4 Watt
V1,V4-4	2			2KΩRes 1/4 Watt
V1,V4-5	2			100ΩRes 1/4 Watt
V1,V4-6	2			470ΩRes 1/4 Watt
V1,V4-7	2			51ΩRes 1/4 Watt
V1,V4-8	2			.1 uF Caps
N.L.	8			2 Amp Pico Fuse
N.L.	2			16 Pin Header
V1,V4,N1,N2,N3	5			

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
±	±	±	
APPROVALS	DATE	ATA Corp.	
DRAWN		COMPUTER IMAGE	
CHECKED		FUNCTION GENERATOR	
		Combiner Board Layout	
		SCALE	SIZE
			B
		DRAWING NO.	010720L1
		DO NOT SCALE DRAWING	SHEET



FG1D7
FG1D6
FG1D5
FG1D4
FG1D3
FG1D2
FG1D1
FG1D0
FG2D7
FG2D6
FG2D5
FG2D4
FG2D3
FG2D2
FG2D1
FG2D0



NOTE: THESE RESISTORS & CAPS AT LOCATION V4
UNLESS OTHERWISE NOTED

NOTE: 2 CIRCUITS PER BOARD

NOTE: $\frac{1}{\perp}$ DENOTES ISOLATED ANALOG GROUND

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

TOLERANCES UNLESS OTHERWISE SPECIFIED			
FRACTIONS	DEC	ANGLES	
$\pm$	$\pm$	$\pm$	
ATA CORP.			
COMPUTER IMAGE			
FUNCTION GENERATOR			
Combiner Board			
APPROVALS	DATE	SCALE	SIZE
DRAWN LPD	7/20/81		B
CHECKED REVA	8/19/81		DRAWING NO.
REV B	11/11/81		010720L1
DO NOT SCALE DRAWING			SHEET 1 of 2

+5P	F.1-20 K.1-30	H.4-16 N.1-16	H.3-2 N.2-16	H.3-4 N.3-16	H.2-16 S.2-9	H.1-14 S.1-9	K.2-30
-GNDP	F.1-10 S.1-10	H.4-8	H.2-8	H.1-7	K.2-32	K.1-32	S.2-10
+15	V.2-7	V.5-7	*Z0-53				
+5	H.4-2 H.2-11	H.4-3	H.4-11	H.3-1	H.3-3	H.2-2	H.2-3
-15	V.2-4	V.5-4	*Z0-55				
-5	S.2-2 V.4-10	S.1-2 *Z0-64	V.1-3	V.1-1	V.1-10	V.4-3	V.4-1
-ANCOM	S.2-17 S.1-8 V.G-8	S.2-5 V.1-13 *Z0-57	S.2-6 V.1-15	S.2-8 V.1-9	S.1-17 V.4-13	S.1-5 V.4-15	S.1-6 V.4-9
-GND	H.4-9 K.1-6	H.2-9	K.2-25	K.2-5	K.2-6	K.1-25	K.1-5
BLDAC1/	F.1-7	H.1-1	K.2-23				
BLDAC21/	F.1-9	H.1-2	K.2-24				
BLDAC23/	F.1-3	H.1-4	K.1-23				
BLDAC3/	F.1-5	H.1-5	K.1-24				
FG1D0	K.2-15	N.2-2	*Z0-97				
FG1D1	K.2-16	N.2-3	*Z0-96				
FG1D2	K.2-17	N.2-4	*Z0-95				
FG1D3	K.2-18	N.2-5	*Z0-94				
FG1D4	K.2-19	N.2-6	*Z0-93				
FG1D5	K.2-20	N.2-7	*Z0-92				
FG1D6	K.2-21	N.3-2	*Z0-91				
FG1D7	K.2-22	N.3-1	*Z0-90				
FG21D0	K.2-26	N.3-9	*Z0-107				
FG21D1	K.2-27	N.3-10	*Z0-106				
FG21D2	K.2-28	N.3-11	*Z0-105				
FG21D3	K.2-29	N.3-12	*Z0-104				
FG21D4	K.2-31	N.3-13	*Z0-103				

FG21D5	K.2-33	N.3-14	*Z0-102
FG21D6	K.2-34	N.3-15	*Z0-101
FG21D7	K.2-35	N.2-9	*Z0-100
FG2D0	K.1-15	N.1-3	*Z0-37
FG2D1	K.1-16	N.1-4	*Z0-36
FG2D2	K.1-17	N.1-5	*Z0-35
FG2D3	K.1-18	N.1-6	*Z0-34
FG2D4	K.1-19	N.1-7	*Z0-33
FG2D5	K.1-20	N.2-1	*Z0-32
FG2D6	K.1-21	N.1-2	*Z0-31
FG2D7	K.1-22	N.1-1	*Z0-30
FG3D0	K.1-26	N.2-15	*Z0-47
FG3D1	K.1-27	N.1-9	*Z0-46
FG3D2	K.1-28	N.1-10	*Z0-45
FG3D3	K.1-29	N.1-11	*Z0-44
FG3D4	K.1-31	N.1-12	*Z0-43
FG3D5	K.1-33	N.1-13	*Z0-42
FG3D6	K.1-34	N.1-14	*Z0-41
FG3D7	K.1-35	N.1-15	*Z0-40
H.1-3	H.4-1	H.1-3	
H.1-6	H.2-1	H.1-6	
H.2-12	H.2-12	S.1-12	
H.2-4	H.2-4	H.2-10	K.1-4
H.3-5	H.4-7	H.3-5	
H.3-6	H.4-15	H.3-6	
H.3-7	H.3-7	H.2-7	
H.3-8	H.3-8	H.2-15	
H.4-12	H.4-12	S.2-12	
H.4-4	H.4-4	H.4-10	K.2-4

K.1-1	K.1-1	S.1-29	
K.1-2	K.1-2	S.1-31	
K.1-3	K.1-3	S.1-33	
K.1-36	K.1-36	S.1-16	
K.1-37	K.1-37	S.1-19	
K.1-38	K.1-38	S.1-23	
K.1-39	K.1-39	S.1-25	
K.1-40	K.1-40	S.1-27	
K.1-8	K.1-8	S.1-35	
K.1-9	K.1-9	S.1-37	
K.2-1	K.2-1	S.2-29	
K.2-2	K.2-2	S.2-31	
K.2-3	K.2-3	S.2-33	
K.2-36	K.2-36	S.2-16	
K.2-37	K.2-37	S.2-19	
K.2-38	K.2-38	S.2-23	
K.2-39	K.2-39	S.2-25	
K.2-40	K.2-40	S.2-27	
K.2-8	K.2-8	S.2-35	
K.2-9	K.2-9	S.2-37	
LDAC1	F.1-14	F.1-13	
LDAC1/	F.1-6	*Z0-98	
LDAC21	F.1-12	F.1-11	
LDAC21/	F.1-8	*Z0-108	
LDAC23	F.1-18	F.1-17	
LDAC23/	F.1-2	*Z0-38	
LDAC3	F.1-16	F.1-15	
LDAC3/	F.1-4	*Z0-48	
S.1-4	S.1-4	V.1-2	V.3-8

S.1-7	S.1-7	V.2-3	
S.2-4	S.2-4	V.4-2	V.6-8
S.2-7	S.2-7	V.5-3	
V.1-12	V.1-12	V.1-11	V.2-2
V.1-14	V.1-14	V.3-2	
V.1-16	S.1-3	V.1-16	
V.1-6	V.1-6	V.3-6	
V.1-7	V.1-7	V.3-4	
V.1-8	V.1-8	V.3-5	
V.3-7	V.1-4	V.3-7	
V.4-12	V.4-12	V.4-11	V.5-2
V.4-14	V.4-14	V.6-2	
V.4-16	S.2-3	V.4-16	
V.4-6	V.4-6	V.6-6	
V.4-7	V.4-7	V.6-4	
V.4-8	V.4-8	V.6-5	
V.6-7	V.4-4	V.6-7	
VCOMB1	V.4-5	V.5-6	*Z0-51
VCOMB2	V.1-5	V.2-6	*Z0-52

TOTAL NUMBER OF WIRE WRAPS: 396

TOTAL PINS USED: 301

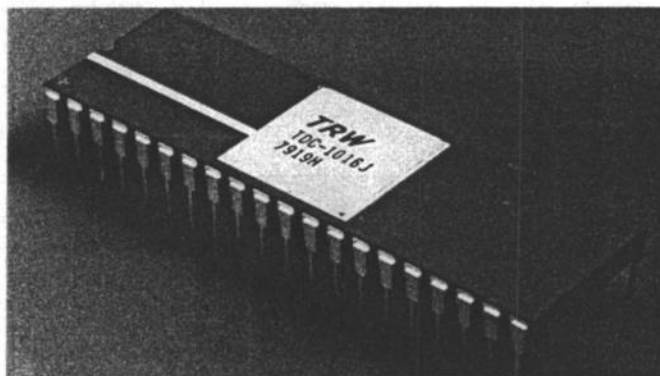
Models: TDC1016J-8
TDC1016J-9
TDC1016J-10

PRELIMINARY INFORMATION

The TRW TDC1016J-8/9/10 bit D/A converters are capable of converting a digital signal into an analog voltage at the rate of 20 megasamples per second (MSPS). No external input register, deglitching, or resampling is needed. No operational amplifier or buffer is required at the analog output.

All parts have 10 bits of active digital input. Three accuracy grades are offered: 8, 9, 10 bits. Simply grounding the V_{CC} terminal causes the inputs to become ECL compatible.

The TDC1016J is patented (U.S. Patent No. 3283170) with other patents pending.

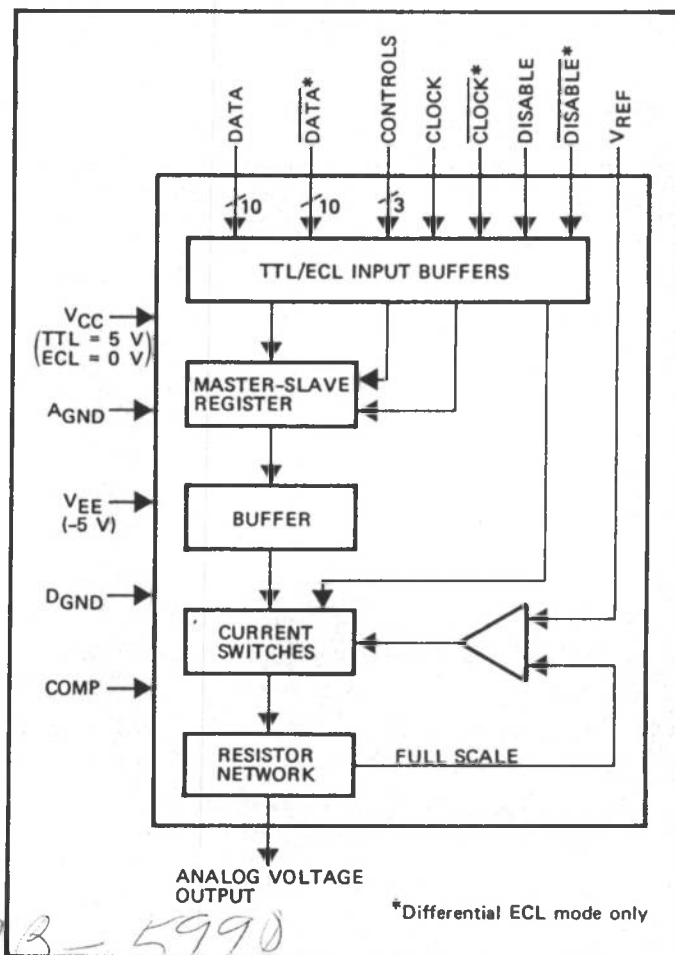


FEATURES

- 8, 9, and 10 bit accuracy
- 20 MSPS
- Voltage output
- ECL or TTL inputs (only -5.0V supply required for ECL mode)
- Single ended or differential ECL inputs
- All data registered on chip
- No deglitching circuit required
- Output disable capability
- Differential phase: 0.5°
- Differential gain: 1.0%
- Binary or two's complement input
- Zero and full scale control for easy calibration
- Data inversion control
- Monolithic, bipolar
- 40 pin ceramic DIP
- 0.6 W power dissipation

APPLICATIONS

- Video data conversion
3X or 4X NTSC color
3X or 4X PAL color
- Color/B&W graphics
- CRT displays
- Waveform/test signal generation



717-518-5990

LSI D/A CONVERTERS

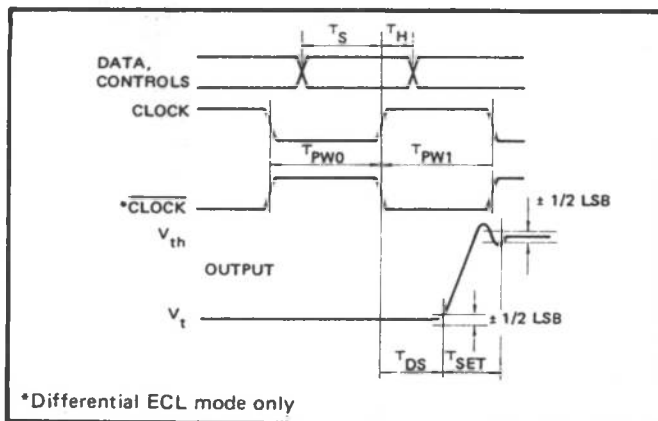


Figure 1. Timing Diagram

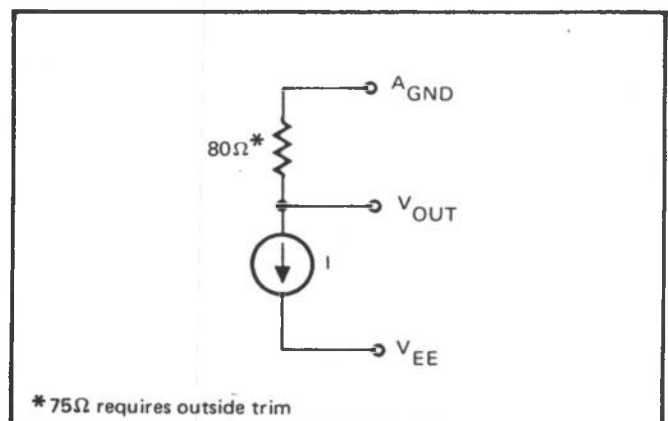


Figure 2. Analog Output Equivalent Circuit, TTL & ECL Mode

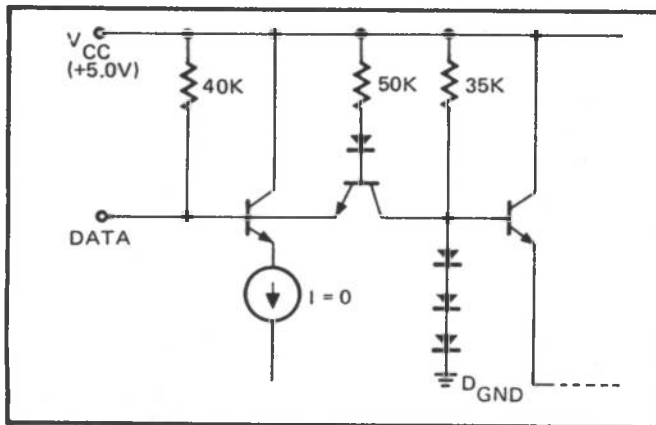


Figure 3. Digital Input Equivalent Circuit, TTL Mode

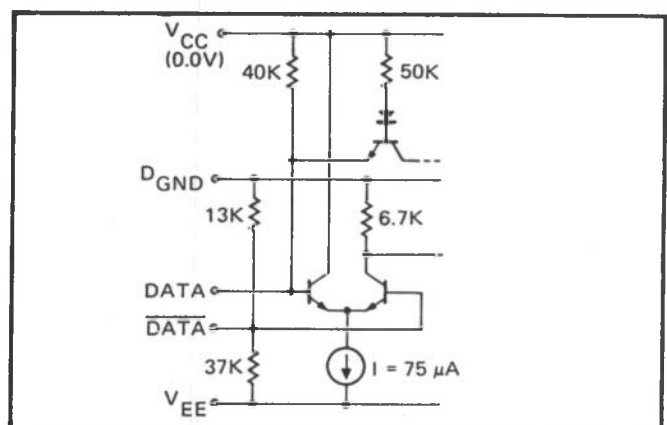


Figure 4. Digital Input Equivalent Circuit, ECL Mode

Performance characteristics, over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TDC1016J-8			TDC1016J-9			TDC1016J-10			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			8			9			10		Bits
			0.39			0.19			0.10		%
Linearity error	0 to 20 MSPS conversion rate			0.20			0.10			0.05	%
Dynamic range	$Z_L > 10K\Omega$	0.8	1.0	1.2	0.8	1.0	1.2	0.8	1.0	1.2	V
	$Z_L = 75\Omega$	0.4	0.5	0.6	0.4	0.5	0.6	0.4	0.5	0.6	V
Output impedance	Resistance	75	80*	85	75	80*	85	75	80*	85	Ω
	Capacitance		5			5			5		pF
Differential phase			0.5			0.5			0.5		Deg
Differential gain			1.0			1.0			1.0		%

*75Ω requires outside trim

LSI D/A CONVERTERS

SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage, V_{CC}	-0.5 to +7.0 V
V_{EE}	+0.5 to -7.0 V
Input voltage, digital	-7.0 to +7.0 V
analog ground	-1.0 to +1.0 V
reference	-7.0 to +7.0 V
Output voltage	-2.0 to +2.0 V
Temperature, operating, ambient	-55 to +150°C
junction	+175°C
lead, soldering (10 seconds)	+300°C
storage	-65 to +150°C

Recommended operating conditions

PARAMETER	TTL			ECL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} , Supply voltage	+4.75	+5.0	+5.25	-0.25	0	+0.25	V
V_{EE} , Supply voltage	-4.75	-5.0	-5.25	-4.75	-5.0	-5.25	V
V_{REF} , Reference voltage	-0.8	-1.0	-1.2	-0.8	-1.0	-1.2	V
τ_{PW1} , τ_{PW0} , pulsewidth (see Figure 1)	15			15			nsec
τ_S , Input register setup time	20			20			nsec
τ_H , Input register hold time	0			0			nsec
T_A , Operating ambient temperature range	0		+70	0		+70	°C
Compensation capacitor (between COMP and V_{EE})	1.0			1.0			μF

Electrical characteristics over recommended operating temperature range

PARAMETER	TEST CONDITIONS	TTL			ECL			UNIT
		MIN	TYP*	MAX	MIN	TYP*	MAX	
Power Supply								
I_{CC} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		10	15				mA
I_{EE} Supply current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}$		100	120		100	120	mA
Analog								
I_{REF} Reference input current	$V_{EE} = \text{MAX}, V_{REF} = -1.0 \text{ V}$		0.1			0.1		μA
V_{OFS} Full scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$	-0.970	-1.0	-1.030	-0.970	-1.0	-1.030	V
V_{OZS} Zero scale analog output voltage	$V_{EE} = \text{NOM}, V_{REF} = -1.0 \text{ V}, R_L > 10K\Omega$			10			10	mV
Digital								
V_{IH} High level input voltage		+2.0			-1.105			V
V_{IL} Low level input voltage				+0.8			-1.475	V
I_{IH} High level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 2.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -0.81 \text{ V}$			75			100	μA
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_{EE} = \text{MAX}, V_I = 0.4 \text{ V}$ $V_{CC} = 0 \text{ V}, V_{EE} = \text{MAX}, V_I = -1.85 \text{ V}$			-0.75			-0.75	mA

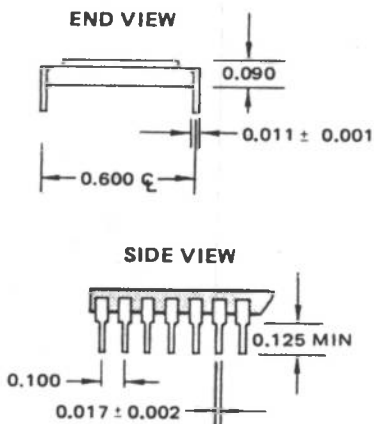
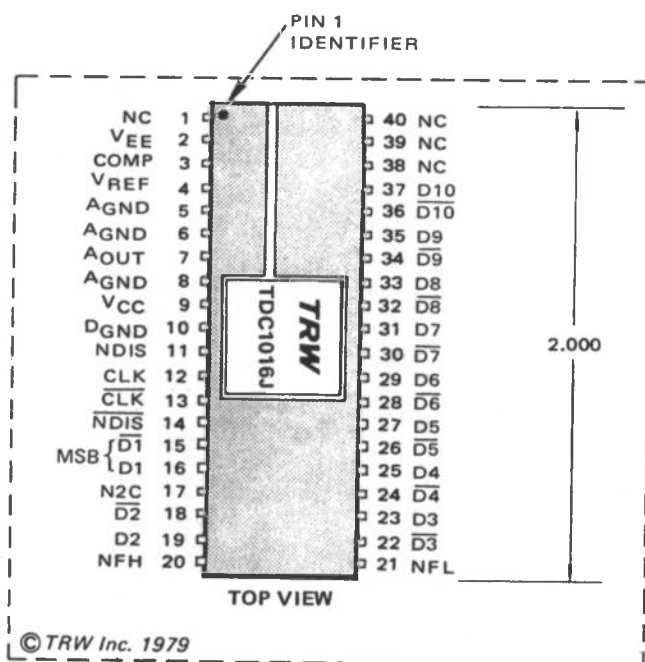
* $V_{CC}, V_{EE}, T_A = \text{TYP}$

Switching characteristics over recommended operating temperature and supply ranges

PARAMETER	TEST CONDITIONS	TTL/ECL			UNIT
		MIN	TYP	MAX	
F_C Maximum conversion rate		20			MSPS
τ_{DOFF} Ladder turnoff delay	$R_L = 75\Omega$			30	nsec
τ_{DON} Ladder turnon delay	$R_L = 75\Omega$			30	nsec
τ_{DS} Data turnon delay, Figure 1	$R_L = 75\Omega$		15		nsec
τ_{SET8} Transient settling time, Figure 1, 0.20%	$R_L = 75\Omega$		20		nsec
τ_{SET9} 0.10%			25		nsec
τ_{SET10} 0.05%			30		nsec
Output transient (glitch), energy amplitude	$R_L = 75\Omega$, midscale		100		pV-sec
			20		mV

LSI D/A CONVERTERS

PACKAGE INFORMATION TDC1016J-8/9/10



THERMAL RESISTANCE DATA

Junction to case	$\theta_{JC} \approx 25^\circ \text{ C/W}$
Case to ambient	$\theta_{CA} \text{ (Still air)} \approx 25^\circ \text{ C/W}$
Case to ambient	$\theta_{CA} \text{ (5 ft/sec airflow)} \approx 15^\circ \text{ C/W}$

NOTES: DIMENSIONS IN INCHES.
UNUSED PINS CAN BE LEFT OPEN.

INPUT CODING

DISABLE NDIS	TWO'S COMPLEMENT N2C	FORCE HIGH NFH	FORCE LOW NFL	INPUT		OUTPUT	FUNCTIONAL DESCRIPTION
				MSB	LSB		
1	1	1	1	1111111111	0000000000	0.0V -1.0V	Default controls
0	x	x	x	xxxxxxxxxx		0.0V	Output disable
1	x	0	1	xxxxxxxxxx	xxxxxxxxxx	0.0V -1.0V	Force high Force low
1	1	0	0	1111111111	0000000000	-1.0V 0.0V	Inverted
1	0	1	1	0111111111	1000000000	0.0V -1.0V	Two's complement
1	0	0	0	0111111111	1000000000	-1.0V 0.0V	Two's complement inverted

x - Don't care

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Model: MPY-8HUI

PRELIMINARY INFORMATION

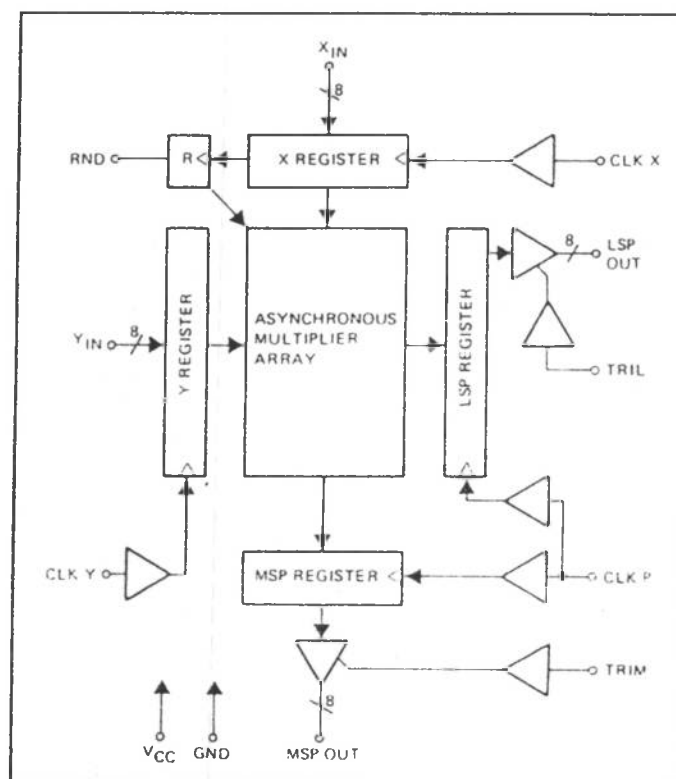
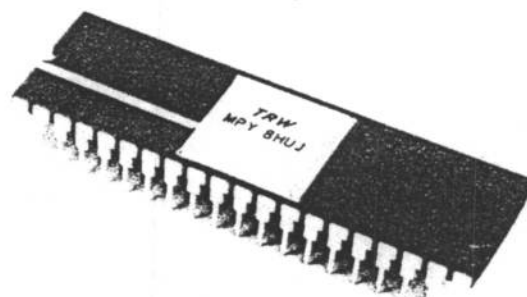
The MPY-8HUI is a high speed, TTL LSI 8 x 8 bit parallel array multiplier, operating on unsigned magnitude inputs, and yielding a double precision product. Its low power and high performance is the result of a proven method developed and patented by TRW (U.S. Patent No. 3,900,724). The main internal multiplier array logic achieves a speed-power performance of less than 0.8 pico-joules per equivalent gate.

Four input and output registers are provided, along with 3-state outputs. These registers are positive-edge triggered D-type flip-flops with independent clocks.

Applications for the MPY-8HUI include digital video signal processing and digital filtering. It is ideal for extending the multiplication capabilities of microcomputers, since all the interface circuitry but the address and clock decoder is included on chip (see page 6). This multiplier is pin-compatible to the MPY8HJ and MPY8AJ, except that it operates on unsigned magnitude numbers, while they operate on two's complement numbers.

FEATURES

- Double precision product
- 45 nanosecond typical multiply time
- Much lower power/less space than MSI equivalent multipliers
- Includes input and output registers
- Single chip, bipolar, TTL
- Single bus or multiport operation
- Radiation hard
- Three-state outputs
- Single power supply, +5V
- Easy interface to microprocessors
- Zero-nanosecond register hold time
- Worst case specs across full voltage and temperature ranges



MPY-8HUU

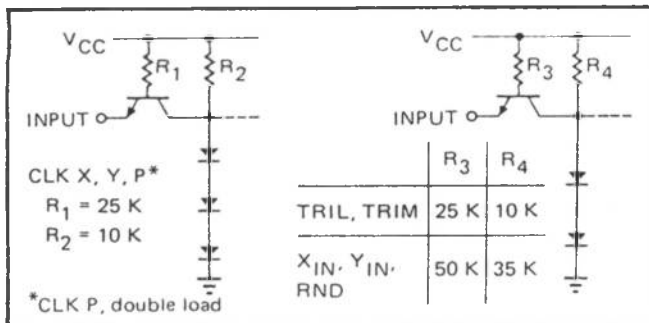


Figure 1. Equivalent Input Schematics

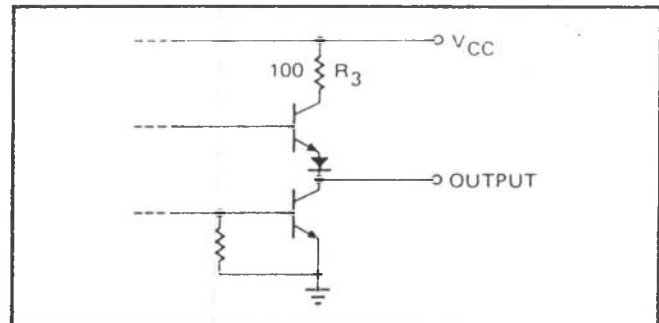


Figure 2. Output Schematic

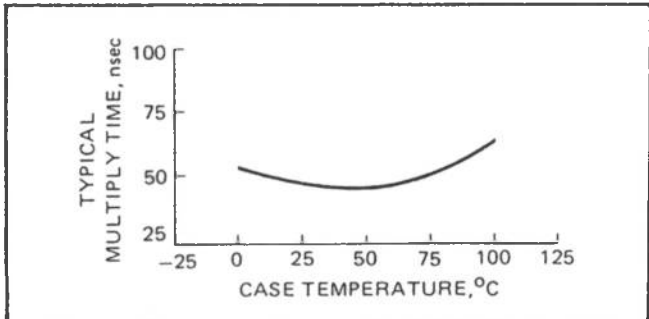


Figure 3. Multiply Time Versus Temperature

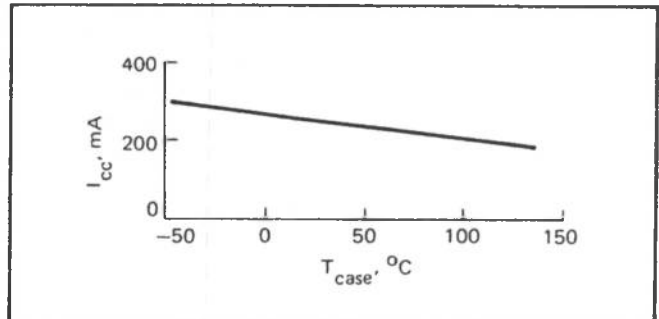


Figure 4. Typical I_{CC} Versus T_{case}

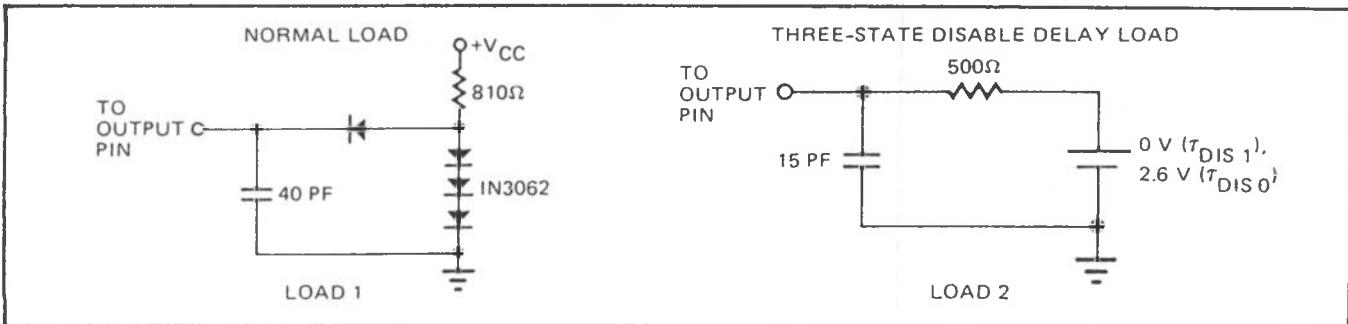


Figure 5. Test Loads for Delay Measurements

SPECIFICATIONS

Absolute maximum ratings (beyond which the useful life may be impaired)

Supply voltage	-0.5 to 7.0 V
Input voltage	0 to 5.5 V
Output voltage	0 to 5.5 V
Operating temperature range (T_{case})	-55°C to 125°C
Storage temperature range	-65°C to 150°C
Lead temperature (10 seconds)	300°C
Junction temperature	175°C

Recommended operating conditions (required for the part to meet published specifications)

	MPY-8HUU MPY-8HUU-1			UNIT
	MIN	TYP*	MAX	
Supply voltage, V_{CC}	4.75	5.0	5.25	V
High-level output current, I_{OH}			-0.4	mA
Clock pulse width, tpw (measured at 1.5 V level)	25			nsec
Input register setup time, t_S (see Figure 6)	25			nsec
Input register hold time, t_H (see Figure 6)	0			nsec
Operating temperature ($T_{ambient}$)	0		70	°C

MPY-8HUU

SPECIFICATIONS

Electrical characteristics over recommended operating temperature ranges

PARAMETER		TEST CONDITIONS	MPY-8HUJ MPY-8HUJ-1			UNITS
			MIN	TYP*	MAX	
I_{IL} - Low level input current	RND, X_{in} , Y_{in}	$V_{CC} = \text{MAX}$ $V_{IL} = 0.4\text{V}$		- 200		μA
	CLKX, CLKY, TRIM, TRIL			- 0.5		mA
	CLKP			- 1.0		mA
I_{IH} - High level input current	RND, X_{in} , Y_{in}	$V_{CC} = \text{MAX}$ $V_{IL} = 2.4\text{V}$		25		μA
	CLKX, CLKY, TRIM, TRIL			25		μA
	CLKP			50		μA
V_{IL} - Low level input voltage						μA
V_{IH} - High level input voltage					0.8	V
V_{OL} - Low level output voltage			2.0			V
V_{OH} - High level output voltage		$V_{CC} = \text{MIN}$ $I_{OL} = 4.0\text{ mA}$ TRIM=TRIL=0 V		0.3	0.5	V
I_{OH} - High level output current		$V_{CC} = \text{MIN}$ $I_{OH} = -0.4\text{ mA}$ TRIM = TRIL = 0 V	2.4	3.1		V
I_{OH} HIZ - High impedance output current		$V_{CC} = \text{MAX}$ $V_{OH} = 2.4\text{ V}$ TRIM=TRIL=5.0 V		25		μA
I_{OL} HIZ - High impedance output current		$V_{CC} = \text{MAX}$ $V_{OL} = 0.4\text{ V}$ TRIM=TRIL=5.0 V		- 25		μA
I_{CC} - Supply current		$V_{CC} = 5.25\text{ V}$ $T_A = 0^\circ\text{C}$				
		$V_{CC} = 5.0\text{ V}$ $T_A = 25^\circ\text{C}$		240		mA
		$V_{CC} = 5.25\text{ V}$ $T_A = 70^\circ\text{C}$				

Switching characteristics over the recommended temperature and voltage ranges

PARAMETER	CONDITIONS	TYP*	MPY-8HUU-1		MPY-8HUU		UNIT
			MIN	MAX	MIN	MAX	
T_{mc} Multiply time	See figure 6	45	10	65	10		nsec
T_o Output delay	Load 1 See figures 5, 6	25					nsec
T_{ENA} 3-state enable time	Load 1 See figures 5, 6	25					nsec
T_{DIS} 3-state disable time	Load 2 See figures 5, 6	20					nsec

*NOTE: At $V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$

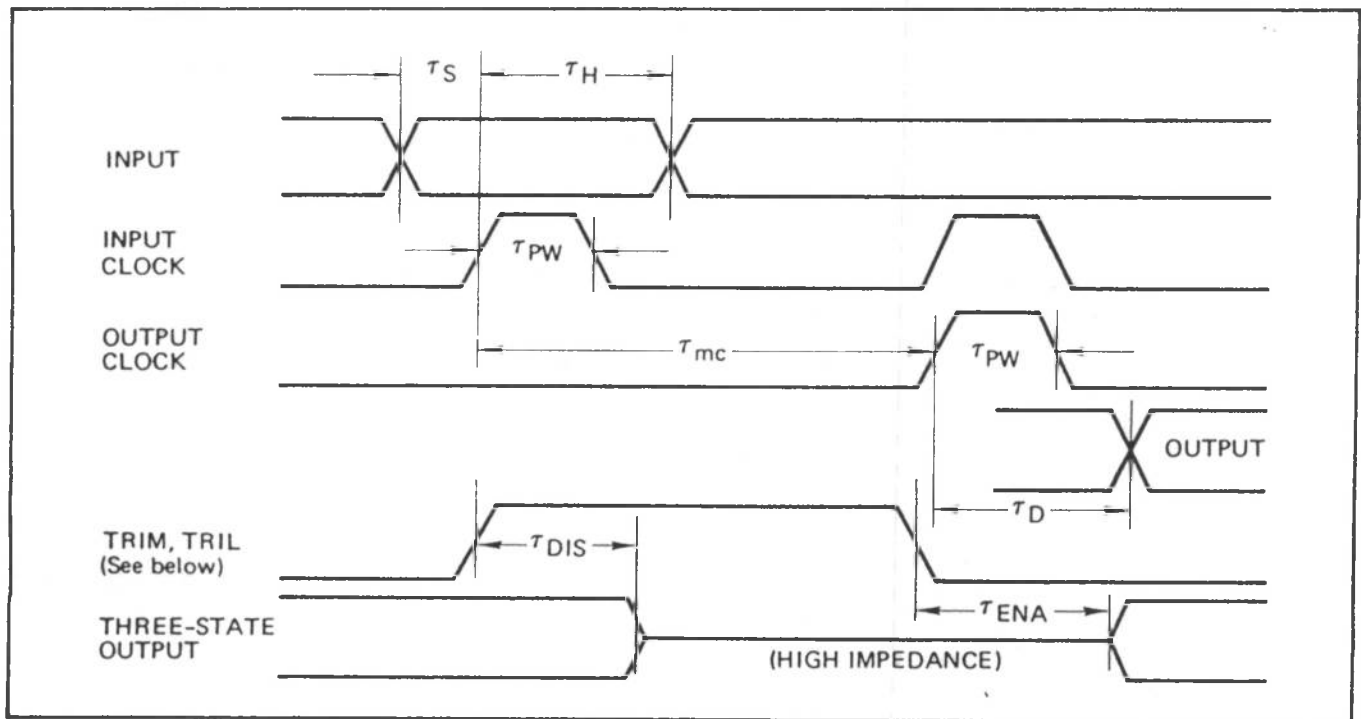


Figure 6. Timing Diagram

GLOSSARY OF TERMS

Commercial temperature range — 0 to 70°C still ambient air, case temperature stabilized under power.

Timing transitions — except for τ_{DIS} , all time measurements are made when a signal crosses 1.5V.

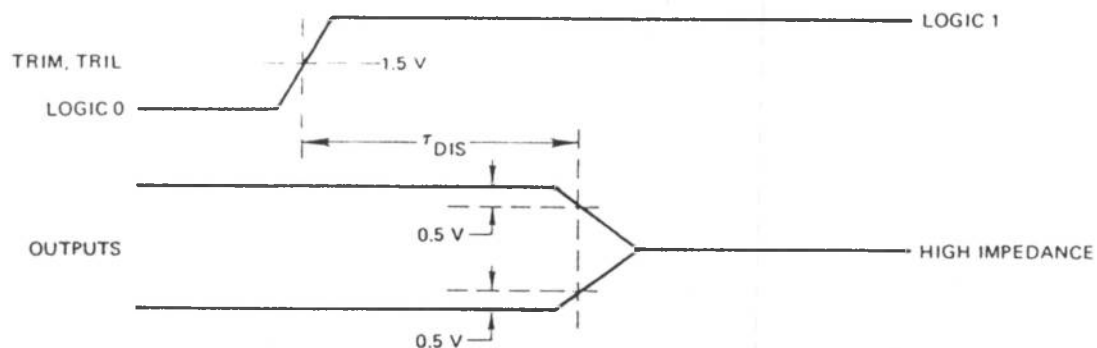
τ_{DIS1} — delay time from a 0 → 1 transition of TRIM or TRIL (measured at 1.5V), until the output pin under test drops 500mV below the previous quiescent logic 1 output voltage (See Figure below).

τ_{DIS0} — delay time from a 0 → 1 transition of TRIM or TRIL (measured at 1.5V), until the output pin under test rises 500mV above the previous quiescent logic 0 output voltage (See Figure below).

X_{in} , Y_{in} — Registered data input ports. X_7 and Y_7 are the MSB, X_0 and Y_0 are the LSB. Data is loaded into the X or Y input registers at the rising edge of CLK X or CLK Y, respectively.

RND — Registered control input, loaded on the rising edge of CLK X. Logic 1 — adds a one to the MSB bit of the LSP output word (P_7), rounding it into the MSP.

TRIM, TRIL — Logic 0 — The output 3-state buffers are enabled to become low impedance outputs.
Logic 1 — The output 3-state buffers are disabled to become high impedance outputs.



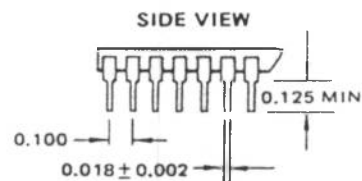
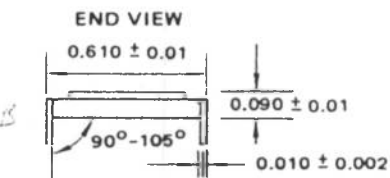
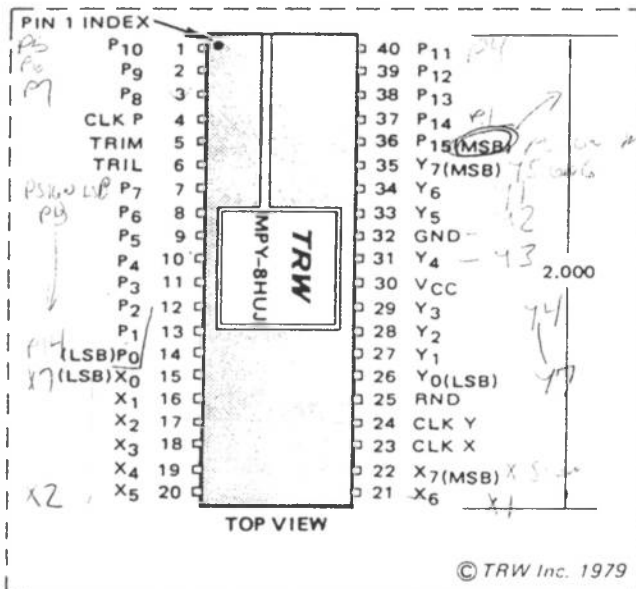
INPUT/OUTPUT FORMAT FOR INTEGER ARITHMETIC

X _{IN}								Y _{IN}							
X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Y ₇	Y ₆	Y ₅	Y ₄	Y ₃	Y ₂	Y ₁	Y ₀
2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
2 ¹⁵	2 ¹⁴	2 ¹³	2 ¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
MSP								LSP							

INPUT/OUTPUT FORMAT FOR FRACTIONAL ARITHMETIC

X _{IN}								Y _{IN}							
X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	X ₇	X ₆	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸
2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶
P ₁₅	P ₁₄	P ₁₃	P ₁₂	P ₁₁	P ₁₀	P ₉	P ₈	P ₇	P ₆	P ₅	P ₄	P ₃	P ₂	P ₁	P ₀
MSP								LSP							

PACKAGE INFORMATION



THERMAL RESISTANCE DATA

Case to ambient θ_{CA} (Still air) $\approx 25^\circ \text{C/W}$
Case to ambient θ_{CA} (300 cfm) $\approx 15^\circ \text{C/W}$

NOTE: DIMENSIONS IN INCHES

SOCKET INFORMATION

TYPE	40 PIN
Wire wrap	Excel 800B-003-40
Solder tail-tin plate	Cambion 703-4040-01-04-12
Solder tail-gold plate	Robinson Nugent ICN-406-S5-G
Zero insertion force	Textool 240-3346-00-0605

MPY-8HUI

The MPY-8HUI is an easy, low power way to upgrade the number-crunching capabilities of a microprocessor. Because the chip comes with input registers and output 3-states, the only other chips necessary are 4 SSI circuits to fully decode the address and generate the interface control signals. Although the chip does have an output register, it can be made transparent to the microprocessor by continuously clocking it — no separate output clock instruction is required. In the application below, the three LSBs of the address bus plus the R/W line are decoded into control signals for the multiplier. Thus, only reads or writes to a small set of addresses are required in the software; the specific instructions are implicit in the addresses. The eight different addresses are given below.

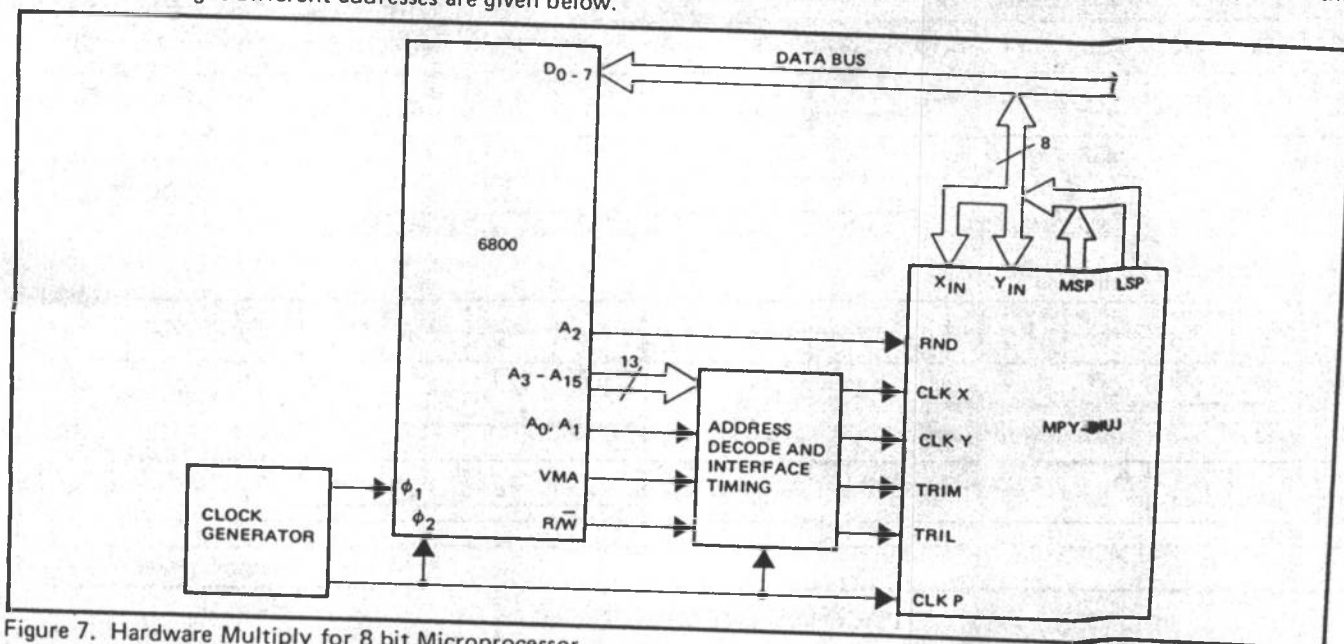


Figure 7. Hardware Multiply for 8 bit Microprocessor

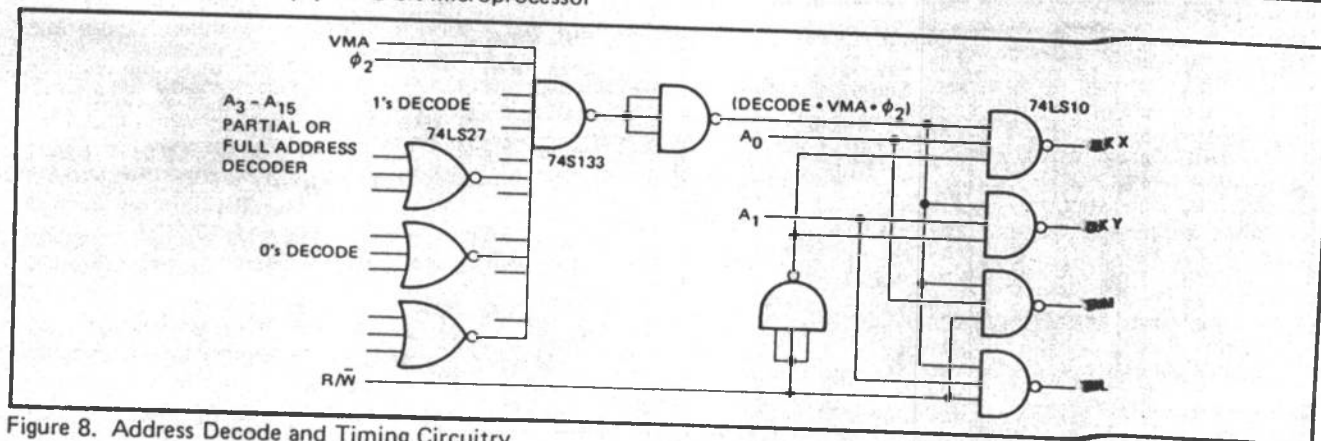


Figure 8. Address Decode and Timing Circuitry

MULTIPLIER INSTRUCTIONS

ADDRESS	WRITE	READ
XXX0	No-op load (interface test)	No-op read (open bus)
1	Load X register, RND = 0	Read most significant product (MSP)
2	Load Y register, RND = 0	Read least significant product (LSP)
3	Load X and Y simultaneous, RND = 0	Do not use! (two 3-bits on at once)
4	No-op load	Same as 0
5	Load X, RND = 1	Same as 1
6	Load Y, RND = 1	Same as 2
XXX7	Load X and Y simultaneous, RND = 1	Same as 3

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